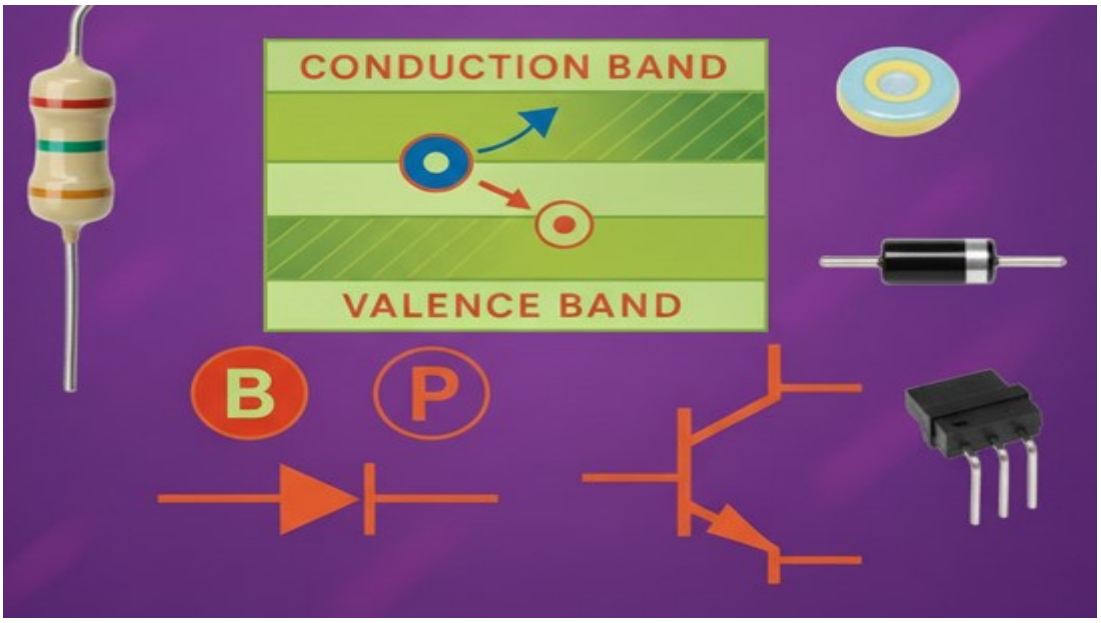
People's Democratic Republic of Algeria
Ibn Khaldoun University of Tiaret
Faculty of Applied Sciences
Electrical Engineering Department

Elements of Physics of Electronic Components



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Course produced using numerous bibliographic references in an educational framework

This comprehensive course covers the physics of semiconductor devices, from theoretical foundations (atomic and crystalline structure) to practical applications (diode, transistor, amplifiers and switches). It is structured progressively, allowing for an in-depth understanding of the essential concepts in microelectronics.

Target audience: Bachelor's and Master's students in electronics, semiconductor physics, and microelectronics.

Table of content

Total numbers of pages: 104
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Chapter I: Generalities on semiconductors

Introduction

At the beginning of our education, in order to understand the phenomena and the nature of matter around us, we asked ourselves many questions such as: what does matter represent? How many states of matter are there? The answer to these questions was three states common to our experience. These states are: solid, liquid and gas. All these states are visible and occur regularly on earth. For example, rocks, ice and trees represent the solid state, water and many oils are liquids, while the atmosphere that surrounds us and we breathe is the gaseous state. However, in addition to these three common states, which are all based on the way atoms are arranged, we can cite another state namely the Plasma state. If an atom is bombarded with sufficient energy, electrons will be torn off and expelled, thus creating an ionized plasma, therefore the fourth state of matter (see figure 1.1).

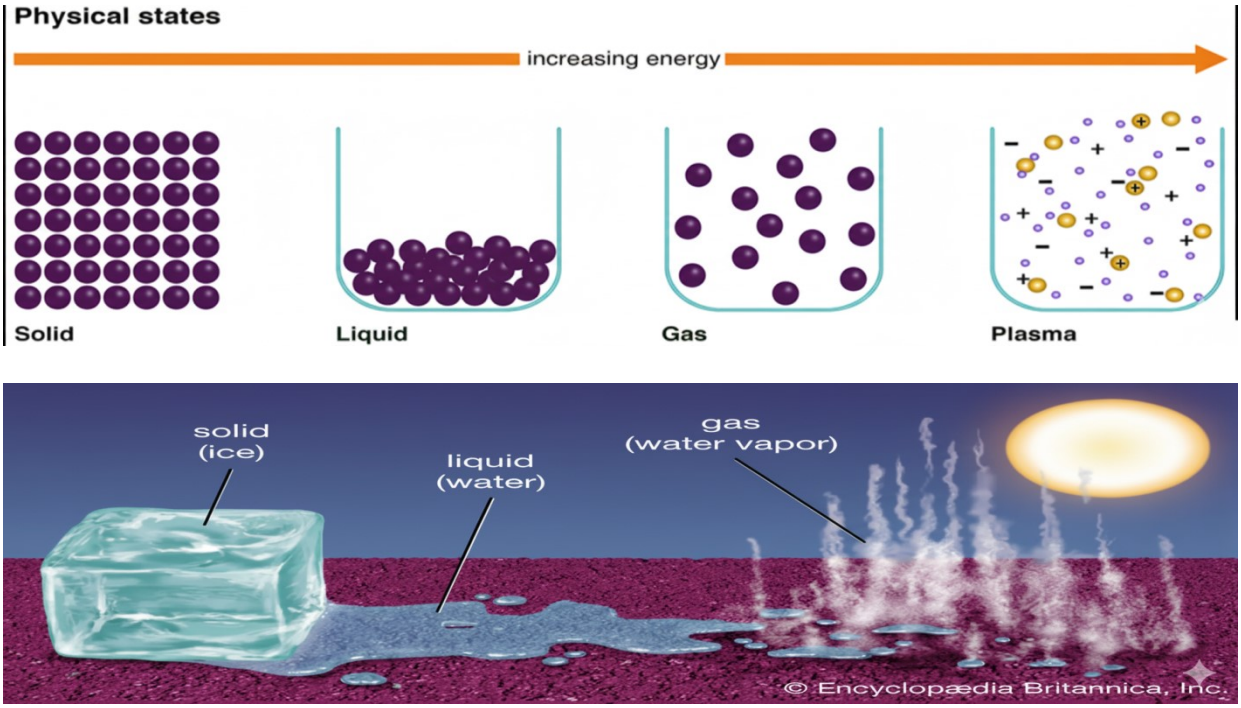


Figure 1.1: The fundamental states of matter

Solids are characterized by an extended three-dimensional arrangement of atoms, ions, or molecules in which the components are usually locked in their positions. Two structures of solids are distinguished:

- **Amorphous structure**: amorphous solids are not arranged in regular lattices or the atoms are organized in a disorderly manner.
- **Crystal structure**: crystalline solids have regular ordered arrays of atoms held together by uniform intermolecular forces. Otherwise, The crystalline state corresponds to an ordered arrangement of atoms or molecules that constitute the solid. There are two types of crystalline solid: Monocrystalline and Polycrystalline.

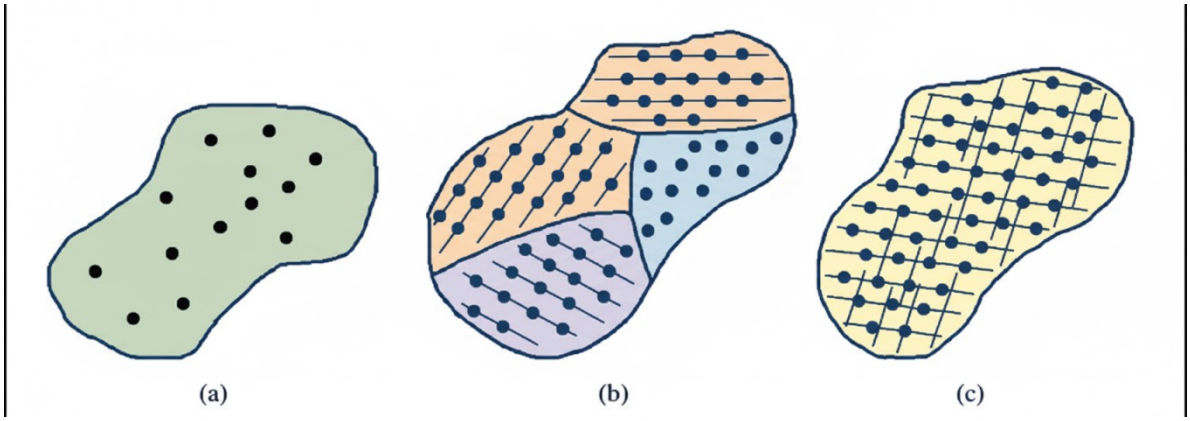
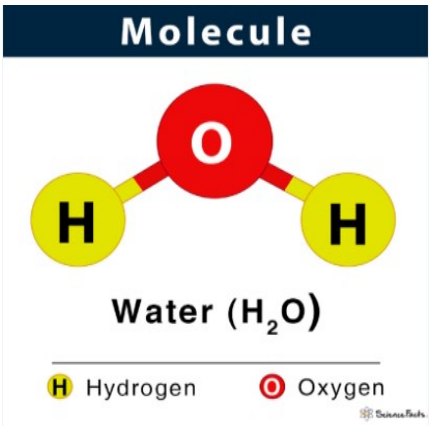


Figure 1.2: Schematic of the three basic structures of crystals: **a)** amorphous, **b)** polycrystalline and **c)** monocrystalline.

Noticed:

In liquid crystals, the order is partial: only the order resulting from the orientation of the molecules is preserved, while the geometric arrangement of the molecules in space is, as in any liquid phase, disordered. All bodies in nature are made up of molecules and atoms.



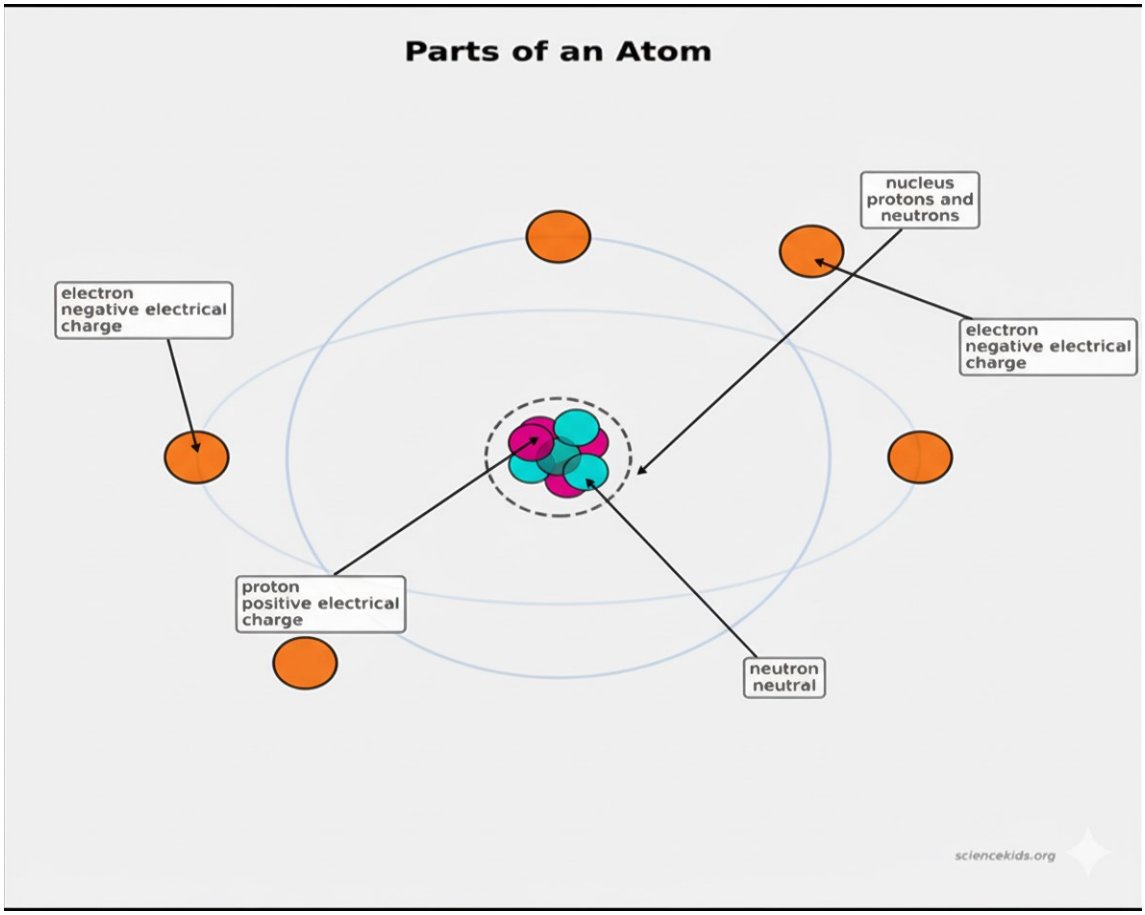


Figure 1.3: Representation of parts of atom

- **The molecule**: is the smallest particle of the body that can be obtained in the free state (around 10-6mm). The molecules are not immobile. A molecule can be monatomic (formed by a single atom). More generally, it will contain several atoms.
- **The atom**: is the smallest particle of an element that can enter into the composition of a molecule.
- **The electron**: is a stable particle of mass: $9{,}109 \times 10^{-28}$g and negative charge equal to $1{,}6 \times 10^{-19}$ Cb.
- **Resistivity**: is the unit that measures the property of bodies to have free electrons in the conduction band. It is expressed in Ohm-meters.

- **Conductivity:** Electrical conductivity or specific conductance is defined as the inverse of resistivity. It is a measure of the amount of electrical current a material can carry or its ability to carry current.

"Conductivity is an intrinsic property of a material."

Based on the order of magnitude of resistivity or conductivity, solid materials can be classified into three categories: conductors, semiconductors, and insulators. In this course we are interested in the physics of semiconductors classified as crystalline solids while detailing their properties and characteristics.

Example: The conductors have a resistivity of the order of μΩ.cm, insulators: 1018Ω.cm and for semiconductors: it is of the order ofΩ.cm

Copper: 1,7x10^{-2}μΩ.cm; Gold: 2,4x10^{-2} μΩ.cm

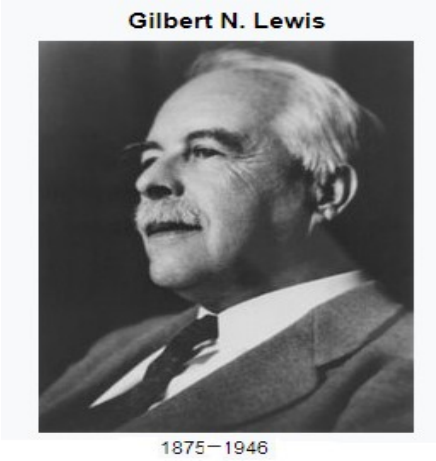
1.1 Atomic bonds

1.1.1 Definition

Chemical bonding is at the very heart of chemistry. Bonding forces determine most of the enthalpy component of the thermodynamic driving forces for reactions and control key features of molecular structure and properties. When two atoms bond together, they can form a molecule. This bond is called a primary bond. Depending on the degree of interaction between the atoms, one of several states can form.

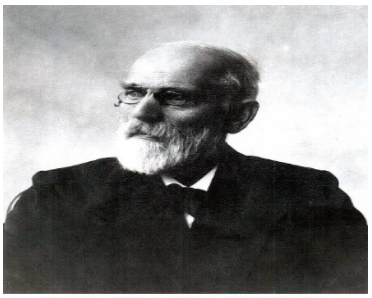
- In the gaseous state: there is little or no resistance to the movement of atoms or molecules.
- In the liquid state: the resistance is much greater but the molecules can move with ease and facility.
- In the solid state: the movement of atoms is restricted to localized vibrations while other movements by diffusion are possible.

1.1.2 Origin of atomic bonds



All bonds have a common origin: the electrostatic attraction between the positive charges of the atomic nucleus and the negative charges of the electrons. There are attractions and repulsions between the electric charges of the electrons and the nuclei. American chemist-physicist **Gilbert Newton Lewis** (1875-1946) played a pivotal role in the development of covalent bond theory. In 1916, he published his seminal paper suggesting that a chemical bond is a pair of electrons shared by two atoms.

The quantum origins of the forces that hold atoms tightly and strongly together have been the subject of intense moved beyond pre-quantum concepts such as "hooks and eyes" to Lewis shared electron pairs. [**Daniel S. Levine1& Martin Head-Gordon**]



The balance between the forces of electrostatic repulsion and attraction leads to the existence of an equilibrium distance between two atoms, characteristic of the bond considered.

1.1.3 Types of atomic bonds

However, for atoms to form crystals, there must be an attractive force between them. This force is called **Van der Waals** attraction. Atomic bonds are of several types. Let us mention the two main ones:

i. **Ionic or electrovalent bond**:

In 1884, Svante August Arrhenius reasoned that an ion is actually an atom carrying a positive or negative charge. He proposed that a compound like sodium chloride would break into ions when dissolved in water, whether or not an electric current was present.

ii. **Ionic bonding:** is based on the effective transfer of one to more than one electron from the outermost layer of the strong metal to the outermost layer of the strong non-metal; the metal is the potential donor of electron(s), the non-metal the acceptor. An ionic combination is the association of ions called **anions** and **cations** which attach to the vicinity of each other by Coulomb attraction.

Ionic bond = strong metal + strong non-metal.

Noticed: **"Strong metal like Cesium and strong non-metal like Fluorine"**. (see Dmitri Ivanovich Mendeleev's periodic table)

Example: Taking the example of Sodium Chloride where chlorine has seven (07) peripheral electrons while sodium only has one.

- **Na^+** as a positive ion since the Sodium atom loses a peripheral electron.
- **Cl^-** as a negative ion because the Chlorine atom recovers the electron torn from the sodium.

- Generally speaking, the loss of an electron by one atom and the gain of an electron by another atom must occur at the same time: for a sodium atom to lose an electron, it must have a suitable receptor, such as a chlorine atom. Each of these atoms ends up with a complete outer shell. It is electrostatic forces that hold the whole thing together.
- Ionic or electrovalent interactions are generally observed in neutralization reactions between acids and bases. Thus, most ionic compounds are salts

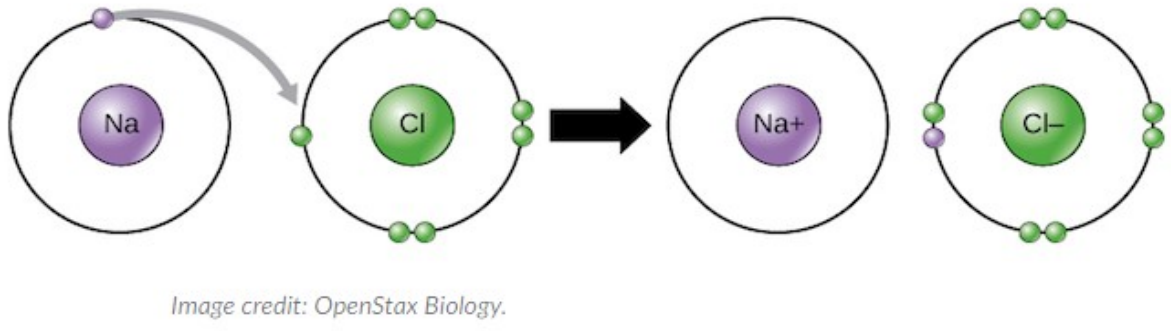


Image credit: OpenStax Biology.

Figure 1.4: Formation of the ionic bond

iii. **Covalent bond**:

Covalent bond = one non-metal + one non-metal.

This is the case for semiconductors and insulators. For silicon, each atom is at the center of a tetrahedron whose four vertices are four other identical atoms. The permitted layers are transformed into bands or zones composed of several distinct but very close layers.

The goal of the covalent bond is to achieve a stable electronic configuration for the two atoms involved. The movement of an electron from one layer to another towards the outside is carried out in a discrete way (by jumps) if additional energy is communicated to it (by heating for example). The return is also possible and is accompanied by a release of energy.

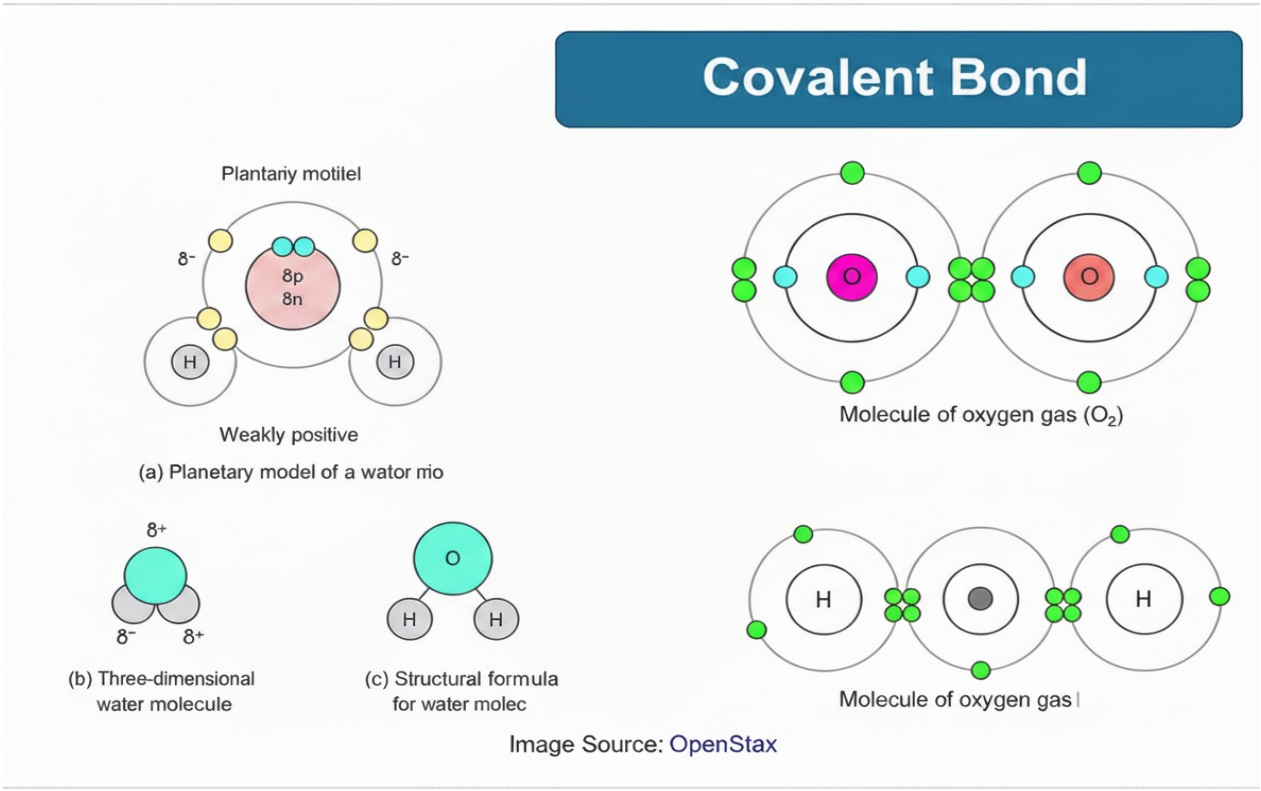


Figure 1.5: Representation of covalent bond

Generally, ionic bonds are much stronger than covalent bonds. In ionic bonds, there is a complete transfer of electrons between elements to form a stable compound. In covalent bonds, there is only one sharing of electrons between two elements to form a stable compound.

1.2 Crystalline solid state

As mentioned above, crystals are a collection of atoms arranged in a certain order. Since the atom is not isolated (it is part of the crystal), its electrons are influenced by neighboring atoms.

1.2.1 Point-lattice

It is made up of a set of points (the green points) placed periodically on which atoms or molecules called: motifs would be placed. Therefore the set point **lattice + motif = crystal lattice**. Examples of motifs include: Silicon (Si), Germanium (Ge) or Galium Arsenide (GaAs) as a binary motif. A crystal lattice is made up of the regular reproduction of a molecule AB or an atom A called: motif or base.

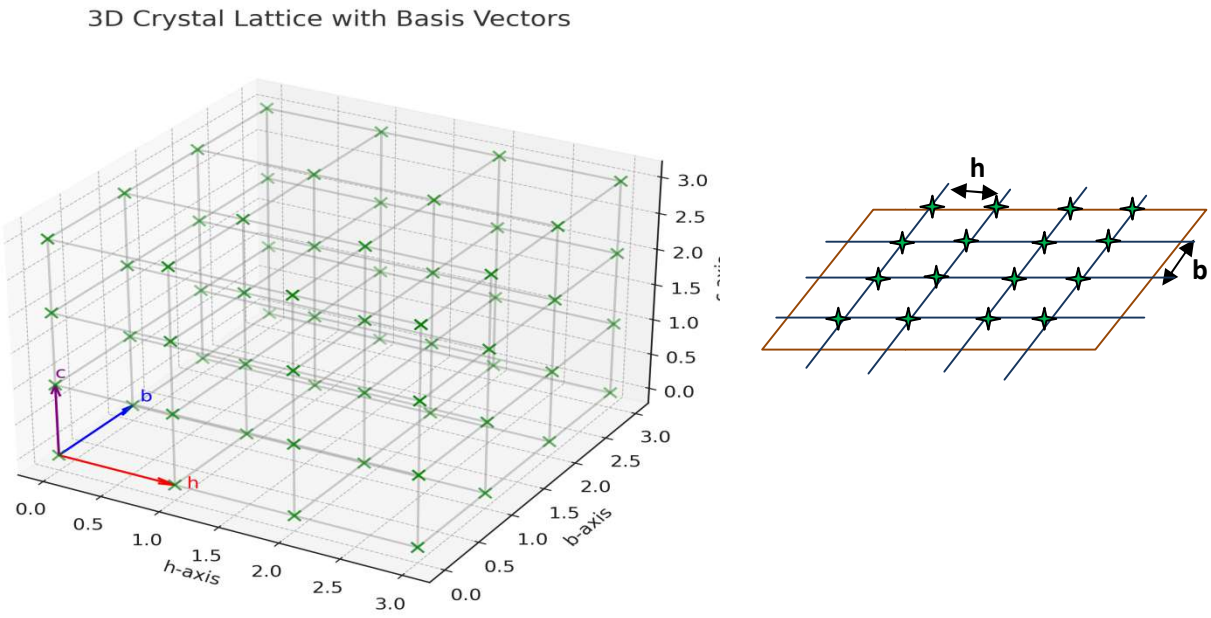


Figure 1.6: Representative diagram of the crystal lattice

1.2.2 Definition

In a crystal lattice we define a reference $(0, \vec{a}, \vec{b}, \vec{c})$. $\vec{a}, \vec{b}, \vec{c}$ are the direction vectors that join two consecutive nodes. The parallelepede formed on these vectors is called an elementary cell. The latter can only contain one node. The node is the smallest part allowing the reconstitution of the crystal. It can be described by the direction vectors $\vec{a}, \vec{b}, \vec{c}$ as well as the angles: α, β, γ. A cell is said to be conventional if it contains at least two nodes

$$\boldsymbol{v_c = v_c.k}$$

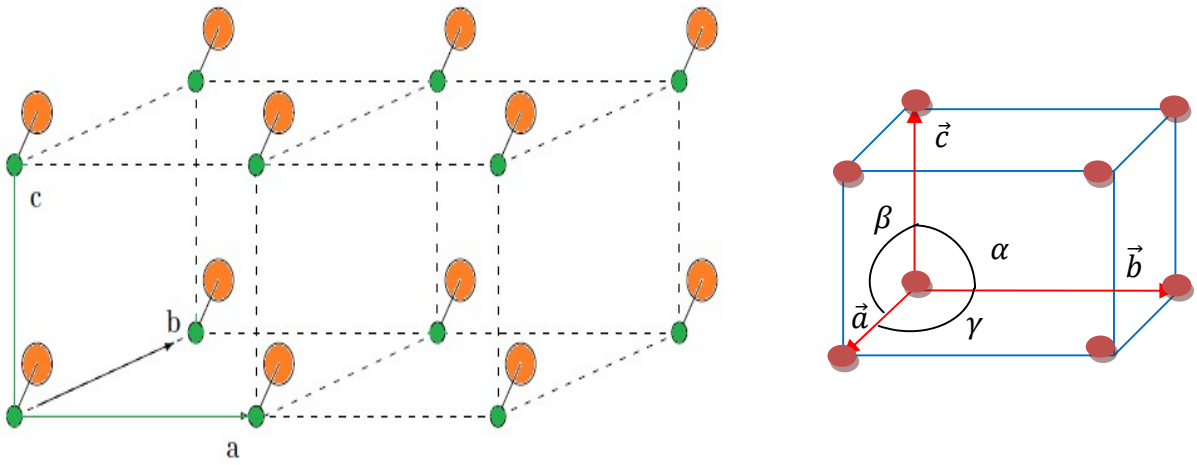


Figure 1.7: Representation of the cubic lattice

1.2.3 The Bravais lattices

In 1948 Bravais demonstrated that three-dimensional space has a lattice number equal to 14 to explain all crystals. They are called direct and are grouped into 7 systems. The primitive lattice, the base-centered lattice, the body-centered lattice and the face-centered lattice are the four types of Bravais lattices. Among these systems, the most important are the cubic, hexagonal and rhombohedral systems. The cubic system is formed by three lattices.

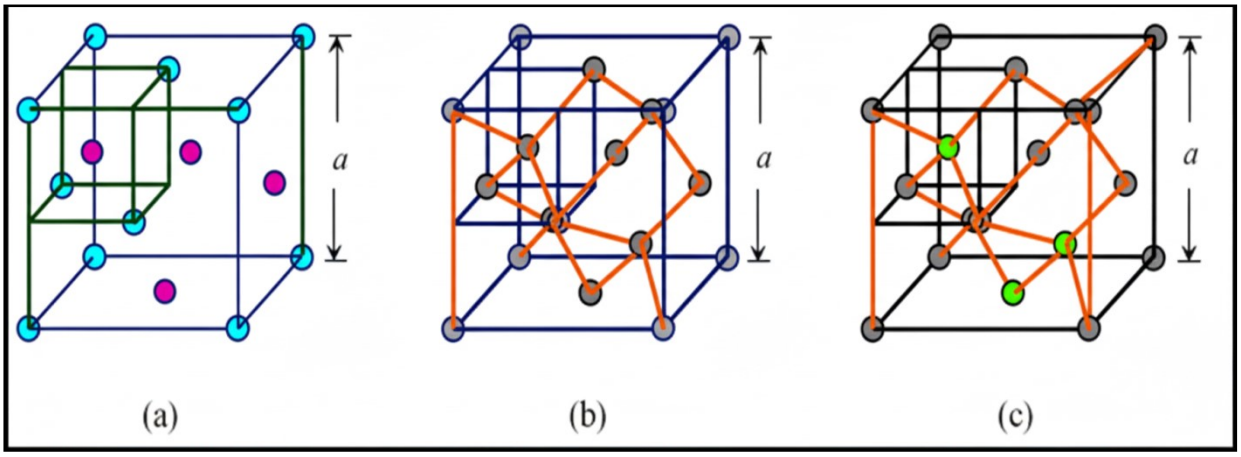


Figure 1.8 a) Face-centered cubic lattice, **b)** Diamond lattice: obtained by moving the lattice atoms of a) by (a/4, a/4, a/4), **c):** Zinc-blend structure: when the displaced lattice atoms are different from the original lattice atoms.

1.2.4 Reticular plane and index

Definition 1: We group all the nodes of a lattice on a plane called the reticular or crystallographic plane.

Definition2: All the nodes can be gathered on a parallel line called a reticular line or crystallographic line.

Definition3: Some families of direction or plans are identified by indices called: Miller indices.

1.2.5 Miller direction indices

Let (a, b, c) be the fundamental vectors of a crystal lattice. If $\vec{v} = h\vec{a} + k\vec{b} + l\vec{c}$, is the crystallographic direction vector. Therefore, the Miller indices are deduced as follows:

$$\vec{v} = -\vec{a} + \frac{3}{4}\vec{b} + \frac{1}{2}\vec{c} \rightarrow \left[1, \frac{3}{4}, \frac{1}{2}\right] \rightarrow \left[-\frac{4}{4}, \frac{3}{4}, \frac{2}{4}\right] \rightarrow [-4,3,2] \rightarrow [4,3,2] \quad \textbf{(1.1)}$$

1.2.6 Miller plan indices

Let be a vector: $v = hx + ky + lz$. The Miller indices of the design are determined as follows:

$$t = 2a + 3b + 4c \rightarrow (2,3,4) \rightarrow \left(\frac{1}{2},\frac{1}{3},\frac{1}{4}\right) \rightarrow \left(\frac{6}{12},\frac{4}{12},\frac{3}{12}\right) \rightarrow (6,4,3) \qquad \textbf{(1.2)}$$

$[a, b, c]$: Miller index of direction
(a, b, c) : Miller index of plan
$< a, b, c >$: Miller index of direction group
$\{a, b, c\}$: Miller index of plan group.

If (h, k, l) are coprime, they characterize the Miller indices of direction or plane or a group of direction or plane. Any index direction $[h, k, l]$ is perpendicular to the plane of the same index (h, k, l).

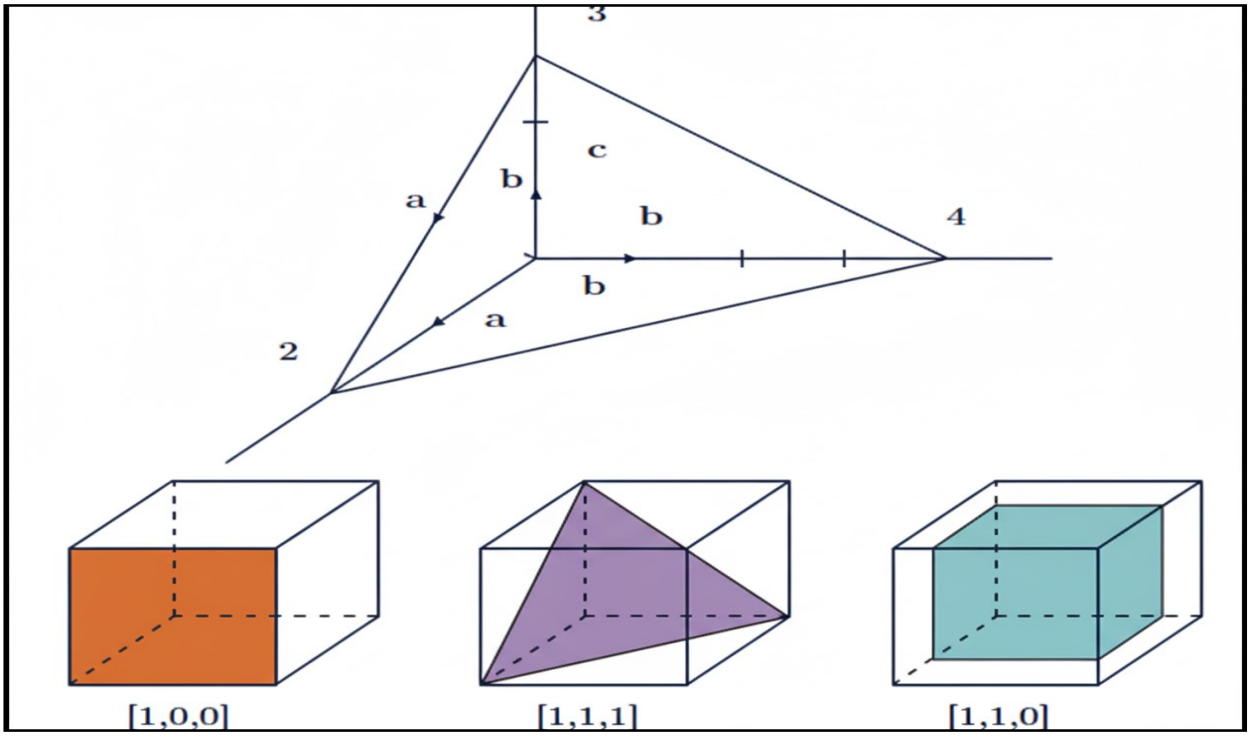


Figure 1.9: Miller indices of the drawn plane & the 3 most common lattice planes for cubic lattices.

1.2.7 Reciprocal lattice

In physics, two lattices are often associated with each crystal structure: direct lattice and reciprocal lattice. The Bravais lattice corresponds to the real space where the fundamental vectors corresponding to lengths are: $\vec{a}, \vec{b}, \vec{c}$. The reciprocal lattice corresponds to the space of wave vectors: $\vec{A}, \vec{B}, \vec{C}$. These represent the reciprocal parameters of the reciprocal lattice. Their dimension is L^{-1} and they are described by the equations below:

$$\vec{A} = \frac{2\pi(\vec{b}\wedge\vec{c})}{\vec{a}.\vec{b}\wedge\vec{c}} \quad \textbf{(1.3)}$$

$$\vec{B} = \frac{2\pi(\vec{a}\wedge\vec{c})}{\vec{b}.\vec{c}\wedge\vec{a}} \quad \textbf{(1.4)}$$

$$\vec{C} = \frac{2\pi(\vec{a}\wedge\vec{b})}{\vec{c}.\vec{a}\wedge\vec{b}} \quad \textbf{(1.5)}$$

1.3 Defects in crystals

The perfect semiconductor single crystal is dull compared to the wide variability of today's deliberately designed materials. The ideal model for a solid requires unintelligible translational symmetry. Each atom resides at its prescribed site; no impurities or defects are permitted. Real crystals are not perfect and have defects. These are sometimes beneficial and introduced deliberately to modify the properties of materials (electrical, optical, crystallographic, etc.). Defects or imperfections in crystalline solids can be divided into four groups, namely point defects, linear (1D or line) defects, surface (2D) defects, and volume (3D) defects.

1.3.1 Point defects

They are involved in certain phenomena such as the diffusion of foreign atoms in crystals. Generally speaking, these defects are generated in metals and ionic crystals.

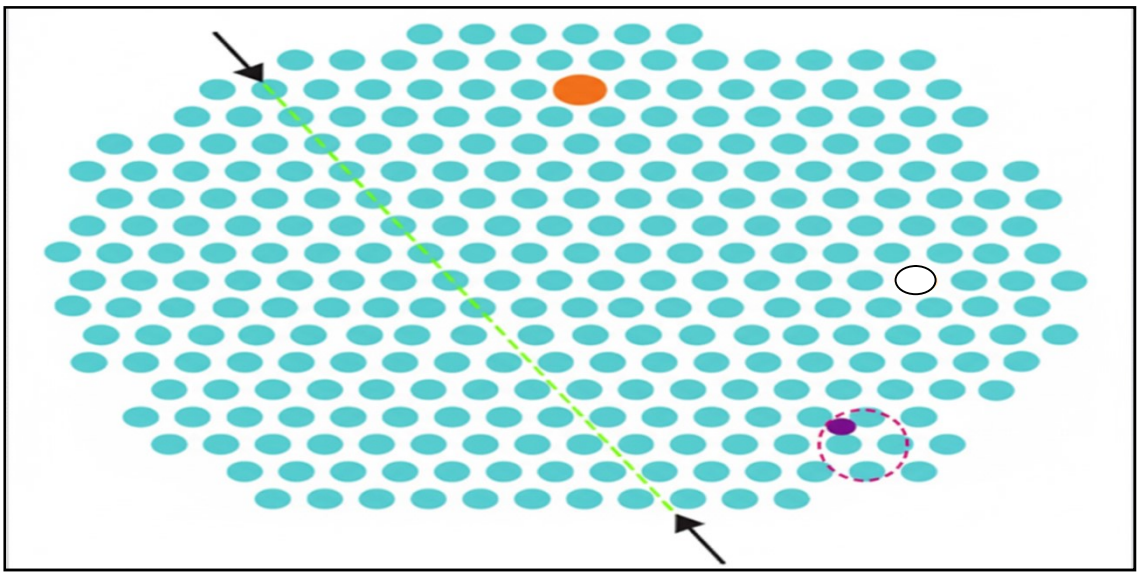


Figure 1.10: Representation of point and line defects

1.3.2 Vacancy and interstitial

A vacancy is the absence of an atom from the crystal lattice, while an interstitial is an atom in the lattice that is no longer in its position. Under the effect of thermal agitation, some atoms acquire sufficient energy to leave their places by tilting neighboring atoms and to accommodate themselves more or less from their defect positions. They would therefore be in an "interstitial" position, commonly called a Fränkel defect.

Noticed: Vacancies can occur without being accompanied by interstitials defects.

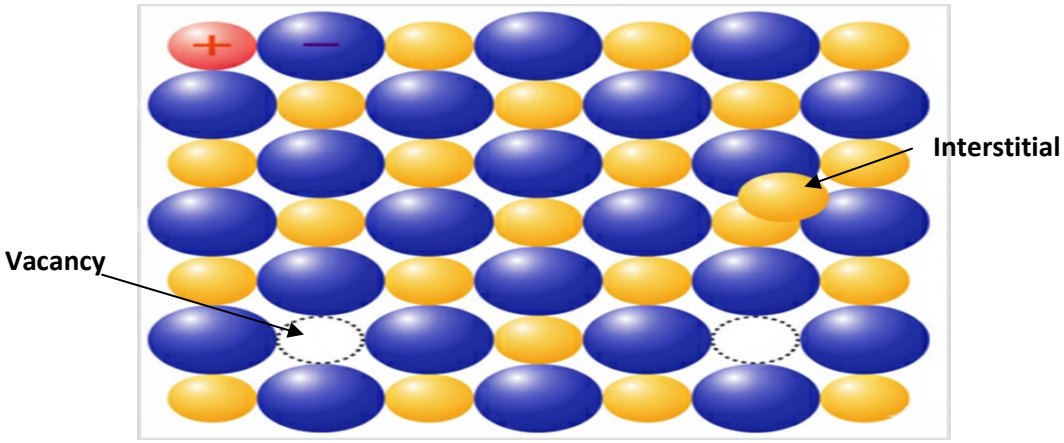


Figure 1.11: Representation of defects: vacancy and interstitial

The presence of two oppositely charged vacancies is called a Schottky defect, while the formation of a vacancy-interstitial pair is called a Schottky defect. Fränkel).

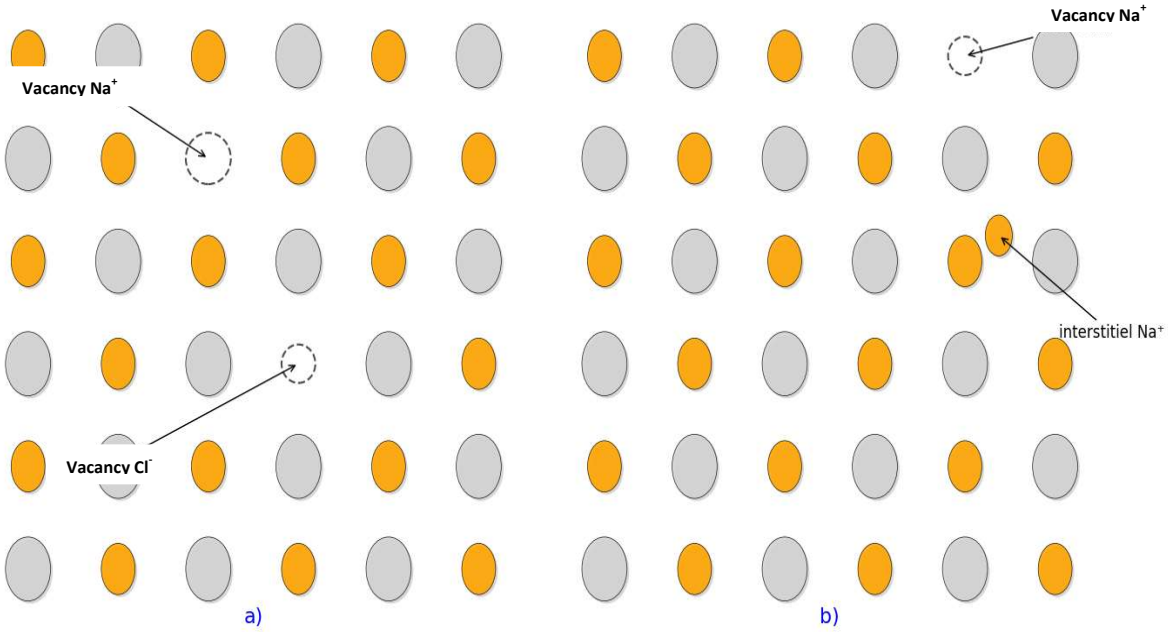


Figure 1.12: Representation of **Fränkel** and **Schottky** defects:

a) Presence of two oppositely charged vacancies (Schottky defect)

b) Formation of a vacancy-interstitial pair (lack of **Fränkel**)

1.3.3 Non-point geometric defects (Dislocations or line)

When a crystal is subjected to pressure, it will undergo deformations which can be: elastic, plastic or fractures. These deformations imply the existence of low resistance surfaces through which the crystallographic planes can slide.

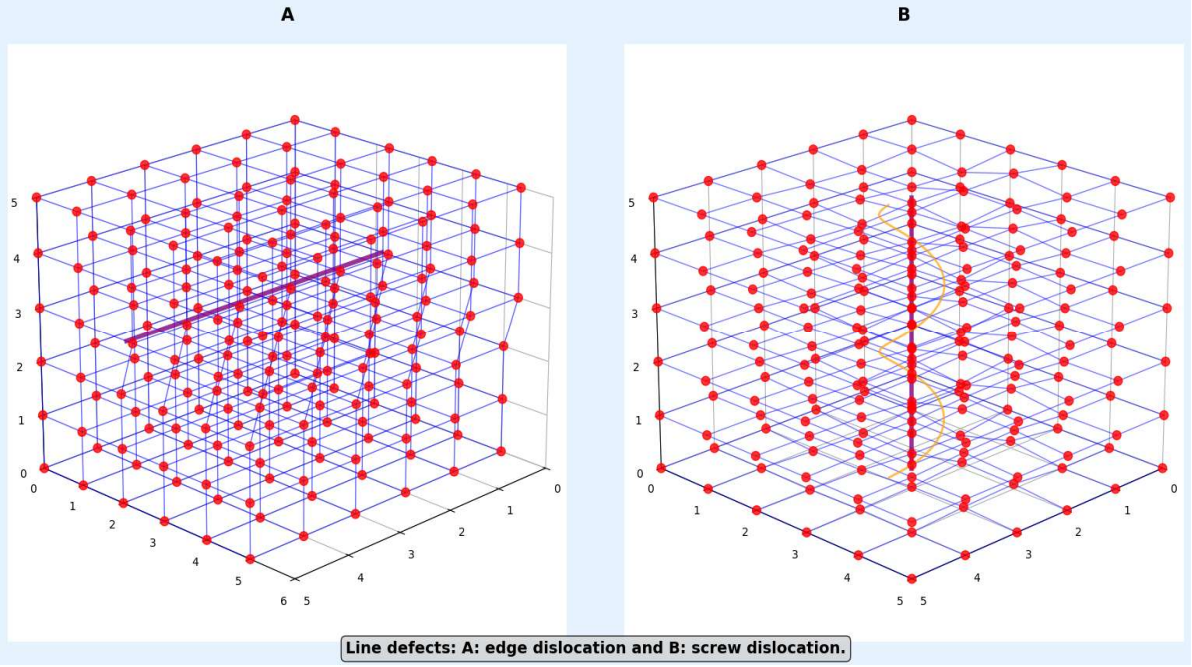


Figure 1.13: Representation of line defects (dislocation)

1.3.4 Composition defects

i. Impurity Defects

These defects are due to foreign atoms incorporated into the crystal in substitution or interstitial positions acting on the properties of the crystal. They must therefore be purified (pure semiconductor is therefore an intrinsic semiconductor).

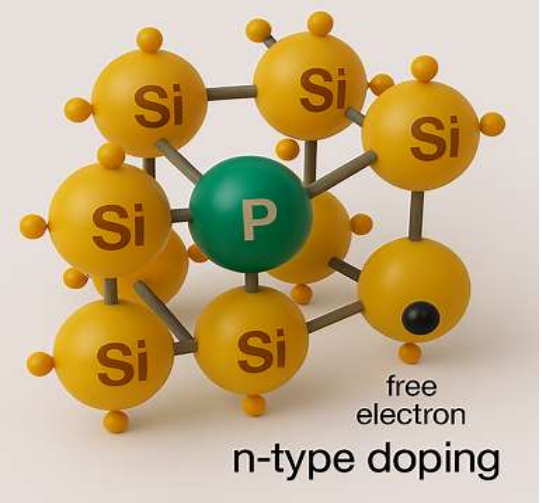
ii. Additive or doping defects

These defects are due to the doping process which subsequently modifies the properties of the crystal, particularly its conductivity. These defects depend on the type of doping: donor or acceptor.

a. Donors

When we introduce donor atoms into a crystal (atoms in the 5^{th} column of the periodic table of materials like Phosphorus and arsenide), the crystal is therefore said to be of type N. In this case (04) electrons of the peripheral layer (last filled layer) form covalent bonds with 04 electrons of silicon. The 5th electron

participates in conduction (by electron). So the donor atoms release an electron into the crystal lattice. The donor atoms create an energy level close to the valence band.



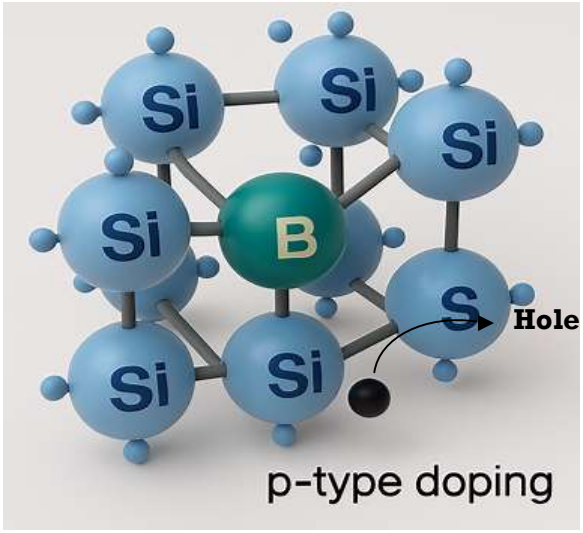
Each phosphorus atom releases an electron into the lattice

Symbol	Name	Atomic Number	Atomic Mass
N	**Nitrogen**	**7**	**14.006855**
P	**Phosphorus**	**15**	**30.973762**
As	**Arsenic**	**33**	**74.92160**
Sb	**Antimony**	**51**	**121.760**

Figure 1.14: Simplified representation of N-type doping

b. Acceptor

When acceptor atoms are introduced into a crystal (silicon for example): atoms from the 3rd column of the periodic table of materials such as Boron or gallium, the crystal is therefore said to be of type P. In this case, three (03) electrons only from the peripheral layer (last filled layer) form covalent bonds with three (03) electrons from silicon. An electron-hole pair is released into the lattice (electron from silicon and hole from Boron). Therefore the acceptor atoms release a hole into the crystal lattice and conduction is done by hole.



Symbol	Name	Atomic Number	Atomic Mass
B	Boron	5	10.81
Al	Aluminum	13	26.9815385
Ga	Gallium	31	69.723
In	Indium	49	114.818

Figure 1.15: Simplified representation of P-type doping

c. Deep defects

In the case of silicon, deep defects appear during the thermal processing of wafers with disordered surfaces. This disorder is the result of mechanical lapping or the introduction of high-concentration impurities into the diffusion layer. Alternatively, deep-level defects are defects positioned deeper in the band gap than dopant levels (shallow donor and acceptor dopants) and bind much more strongly to carriers in tightly packed localized states. Deep levels have higher ionization energies and therefore contribute very little to free charge carriers.

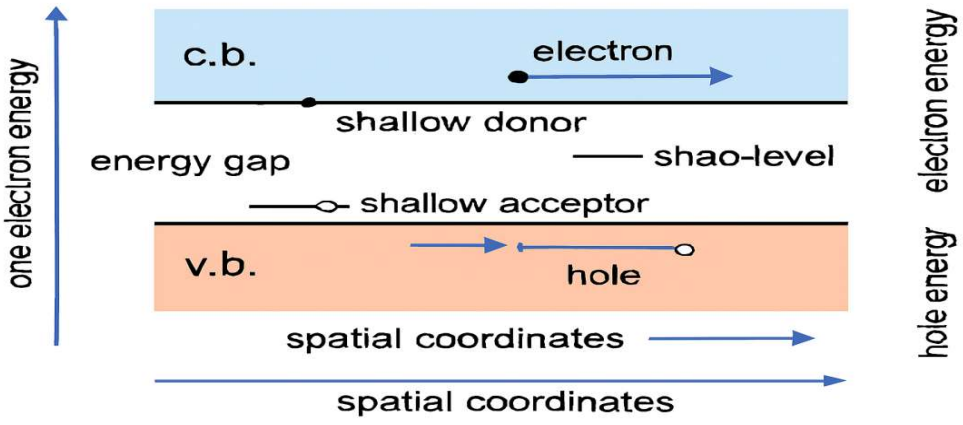


Figure 1.16: Schematic representation of the energy levels created by deep defects and by dopants.

1.4 Energy band theory in crystals

The study of band theory aims to understand the electrical properties of free charges. In this section, we will outline the principles related to energy bands for an isolated atom and an atom in the crystal lattice. In order to calculate the energy band structures of a semiconductor, it is necessary to:

- Calculate the first Brillouin zone.
- Calculate the energy band structures in the limit of zero potential energy.
- Then calculate the energy bands using an appropriate method.

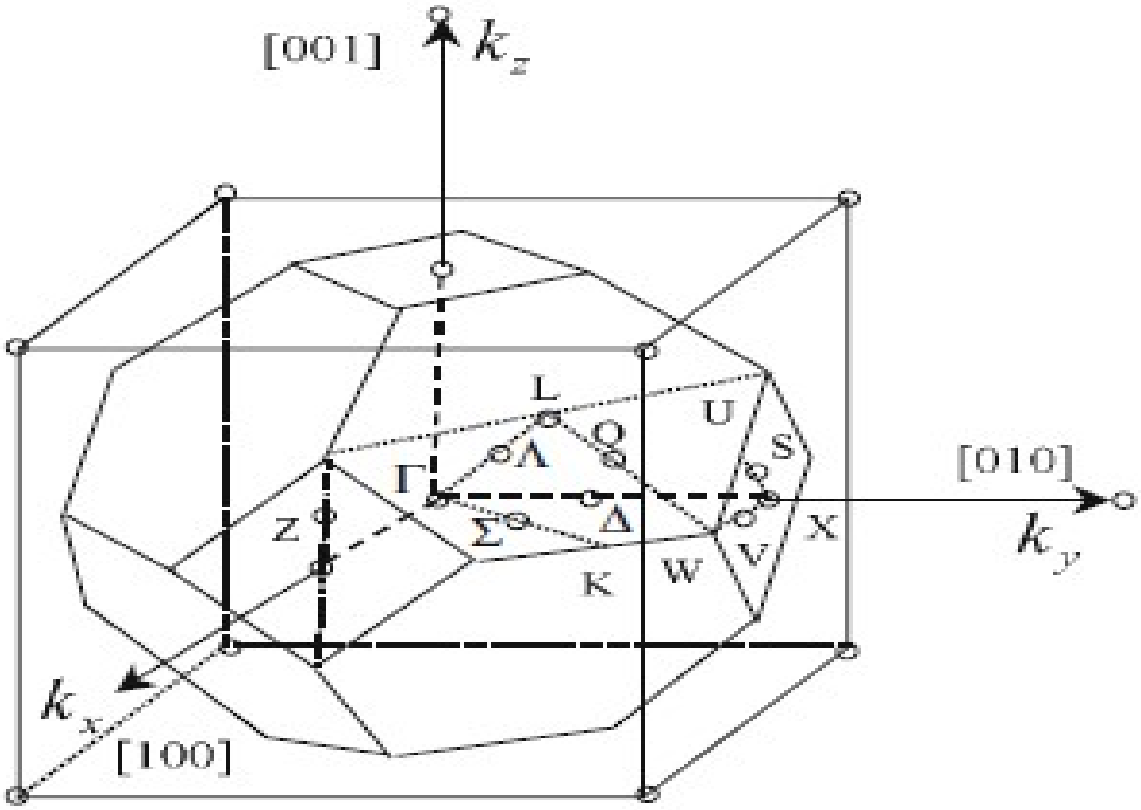


Figure 1.17: Brillouin zone of a face-centered cubic lattice.

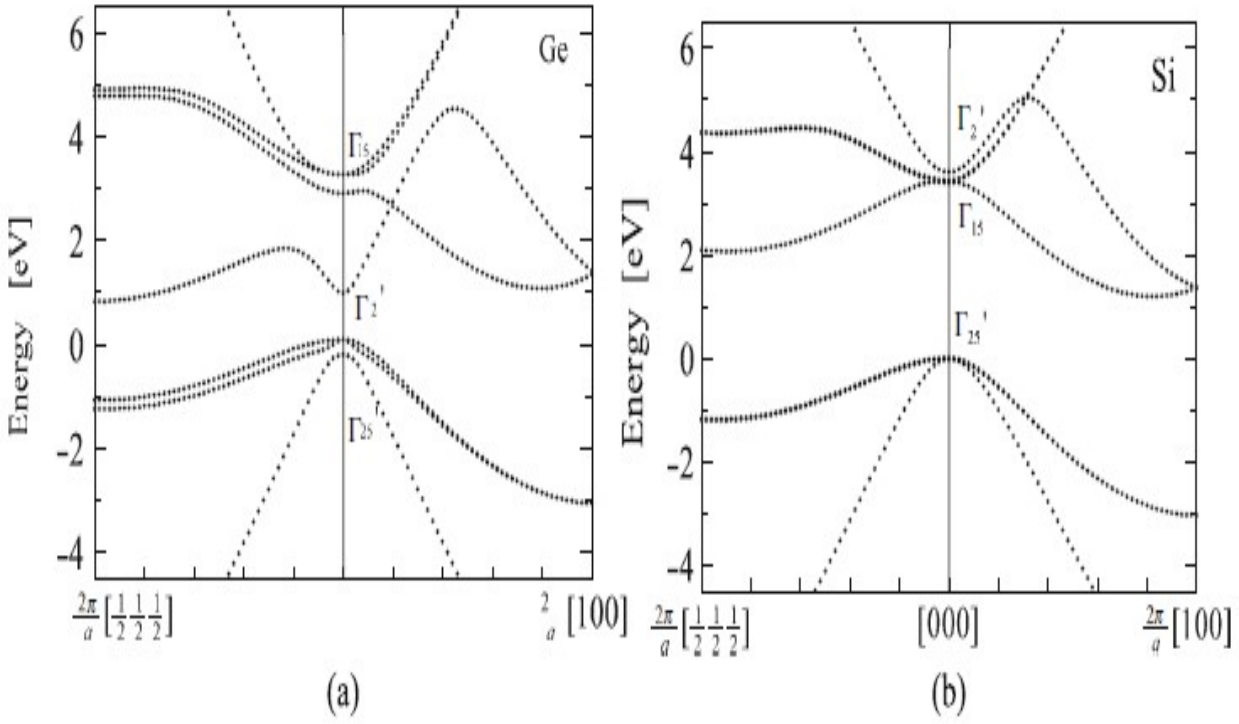


Figure 1.18: Examples of energy band structures calculated by the K.p perturbation method: a) Germanium b) Silicon

1.5 Energy bands and level density

1.5.1 Electrical analogy: LC circuit

Consider the LC circuit in the figure opposite. We propose to determine the oscillation frequency of the circuit.

$$\frac{q}{c}+\frac{q}{c_1}+L\frac{d^2q}{dt^2}=0 \qquad \textbf{(1.6)}$$

The solution is of the form: $q(t)=Ksin(wt+\varphi)$

$$\left(Lw_0^2-\frac{1}{c}+\frac{1}{c_1}\right)q=0 \;\rightarrow\; w_0=\sqrt{\frac{1}{L}(\frac{1}{c}+\frac{1}{c_1})} \qquad \textbf{(1.7)}$$

2nd case:

$$\begin{cases} L\frac{d^2q_1}{dt^2}+\frac{q_1}{c}+\frac{q_1+q_2}{c_2}=0 \\ L\frac{d^2q_2}{dt^2}+\frac{q_2}{c_1}+\frac{q_1+q_2}{c_1}=0 \end{cases} \qquad \textbf{(1.8)}$$

With: $q_1 = A_1 \sin(wt + \varphi_1)$, $q_2 = A_2 \sin(wt + \varphi_2)$

$$\begin{cases} \left(-L\omega^2 + \frac{1}{c} + \frac{1}{c_1}\right) q_1 + \frac{q_2}{c} = 0 \\ \left(-L\omega^2 + \frac{1}{c} + \frac{1}{c_1}\right) q_2 + \frac{q_1}{c} = 0 \end{cases} \quad \textbf{(1.9)}$$

q_1 and q_2 are the roots of the system, the only solution is $q_1 = q_2 = 0$, or $q_1 \; and \; q_2 \neq 0$, so it is the determinant is equal to 0.

$$\left(-L\omega^2 + \frac{1}{c} + \frac{1}{c_1}\right)^2 = \left(\frac{1}{c_1}\right)^2 \rightarrow L\omega^2 = \frac{1}{c} + \frac{1}{c_1} \pm \frac{1}{c_1} \quad \textbf{(1.10)}$$

So $$\omega^2 = \omega^2{}_0 \pm \frac{1}{Lc_1}, \; w_0^2 = \frac{1}{Lc} + \frac{1}{Lc_1} \quad \textbf{(1.11)}$$

The simple LC circuit oscillates with a single frequency, if it is added to another circuit there will be a 2nd frequency. The oscillation frequency of the electrical system is analogous to the electrical energy in another.

1.5.2 The energy levels of electrons in the isolated atom

In an isolated atom, electrons can only occupy discrete energy levels. The electrons occupy circular orbits of radius r_n to which potential energies V are associated (crystalline potential). These electrons occupy the orbits closest to the nuclei. The electrons in the outermost shell are the valence electrons least bound to the nucleus.

$$r_n = n^2 \varepsilon_0 \frac{ln^2}{\pi m q^2} \quad \textbf{(1.12)}$$

$$V_c(r) = V_c(r + T) \quad \textbf{(1.13)}$$

$$V = \frac{q^2}{4\pi\varepsilon_0 r} \quad \textbf{(1.14)}$$

With T represents the translation vector of the crystal lattice.

The periodicity of the crystal potential results in a fundamental property of the electron wave function given by the ***Bloch's theorem.***

1.5.3 Energy structure of the crystal

a. Definition

In a crystal, electrons are arranged in a perfectly periodic manner; they are not independent but coupled instead of each single level of the isolated atom. We have "n" energy levels.

2 The valence band (VB): this is the last permitted energy band occupied by electrons at (0K)

3 The conduction band (CB): this is the first empty band of electrons at (0K). When passing from the CB to the CB, the electron leaves behind a hole.

The energy band that separates the valence band from the conduction band is called the forbidden band or gap characterized by an energy $\mathbf{E_g}$. This energy allows us to classify it as a semiconductor, insulator or conductor.

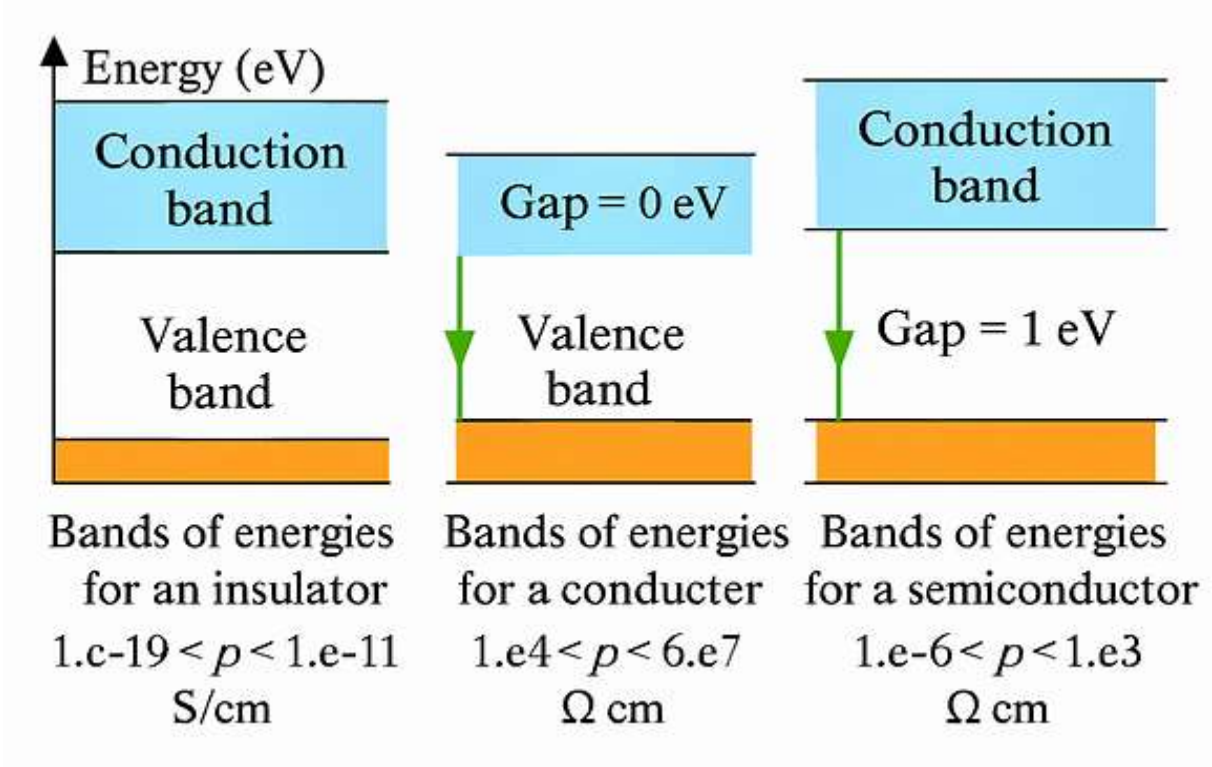


Figure 1.19: Representation of energy bands in an insulator, conductor and semiconductor.

b. Notion of hole

In a semiconductor material, at temperature of **zero Kelvin**, all electrons are in the valence band. The material is considered an insulator. If the temperature increases, the electrons can reach the BC. In this case, the electrons leave in their place voids called holes. The latter are positively charged and can be occupied by other electrons. We talk of hole conduction in the valence band and electron conduction in the conduction band. Let the crystals contain "**n**" atoms at a particular possible energy whose isolated atom will correspond to a group n of possible energies which are all the more important than the initial level as the interaction between the electrons is strong. The possible energies for an electron in a solid form permitted bands (PB) separated by forbidden bands.

c. Density of levels in a permitted band

For an electron to move from the valence band to the conduction band, it must be supplied with energy $\geq E_g$, and D_E which is defined as the level density. It is zero outside the permitted bands. For an atom isolated in space, the energy levels of its different electrons are perfectly determined by the quantum numbers N, L, M. In accordance with the "**Pauli exclusion principle**", each level can be occupied by only two electrons, with opposite spins. In a crystal, the energy levels are then divided into AA permitted bands′, BB′, intervals such as A′B′ being forbidden bands. In this bringing together of atoms and the decomposition of levels, it may happen that the allowed bands overlap or not.

Chapter II: Electronic transport in semiconductors

Introduction

The study of electronic transport in semiconductors and solids in general is essential in determining the electrical properties of both semiconductors and components. Transport is an intrinsically non-equilibrium phenomenon, where the role of dissipation and coupling to the environment play a crucial role. In this chapter, we discuss the charge transport mechanisms and the different currents flowing in a semiconductor.

2.1. Population of energy levels: at thermodynamic equilibrium

Knowing the band structure as well as the localized quantum levels (introduced into the band gap by impurities), it would be necessary to determine their distribution across the authorized energy levels (the allowed bands) while evaluating the conductivity of electrons and holes. However, knowledge of the position and the exact kinetic energy associated with each electron remains impossible. For this we resort to statistical methods and probability laws.

2.1.1. Concepts of probability of occupation of an energy level E

According to the Pauli exclusion principle there can only be 1 or 2 electrons per quantum level. Given the Pauli exclusion principle, we must therefore know what probability $f(E)$ exists for a crystal electron to have occupied an energy level E. In static thermodynamics it is shown that for the electrons of the crystal we can apply the Fermi-Dirac statistics.

According to this statistic, the electrons of a crystal are assimilated to an electronic gas such that:

$$f(E) = \frac{\textit{nombre de places occupées}}{\textit{nombre de palces occupables}}$$

2.1.2. In the case of electrons

$$f_n(E) = \frac{1}{1 + \exp\left(\frac{E - E_F}{KT}\right)} \quad \textbf{(2.1)}$$

$f_n(E)$: Probability that an energy level E is occupied by an electron at thermodynamic equilibrium.

E_F :is a reference level called the Fermi level defined as the last occupied level at 0K.

K = 8,62 x10^{-5}eV/K is the Boltzmann constant and T temperature in Kelvin (K)

2.1.3. In the case of holes

The probability function that an energy level E is occupied by a hole is given by the following expression:

$$f_p(E) = 1 - f_n(E) = 1 - \frac{1}{1 + \exp\left(\frac{E - E_F}{KT}\right)} \quad \textbf{(2.2)}$$

$$f_p(E) = \frac{1}{1 + \exp\left(\frac{E_F - E}{KT}\right)} \quad \textbf{(2.3)}$$

The fundamental nature of the distribution function dictates that at ordinary temperatures, most levels up to the Fermi level E_F are filled, and relatively few electrons have energies above the Fermi level.

The Fermi level is on the order of electron volts, whereas the thermal energy "**KT**" is only about 0,026 eV at 300K. So if we put these numbers into the Fermi function at ordinary temperatures, we find that its value is essentially 1 up to the Fermi level and quickly approaches zero above it.

The illustration below shows the implications of the Fermi-Dirac function for the electrical conductivity of a semiconductor. The band theory of solids shows that there is a large gap between the Fermi level and the conduction band of the semiconductor. At higher temperatures, a larger fraction of electrons can bridge this gap and participate in electrical conduction.

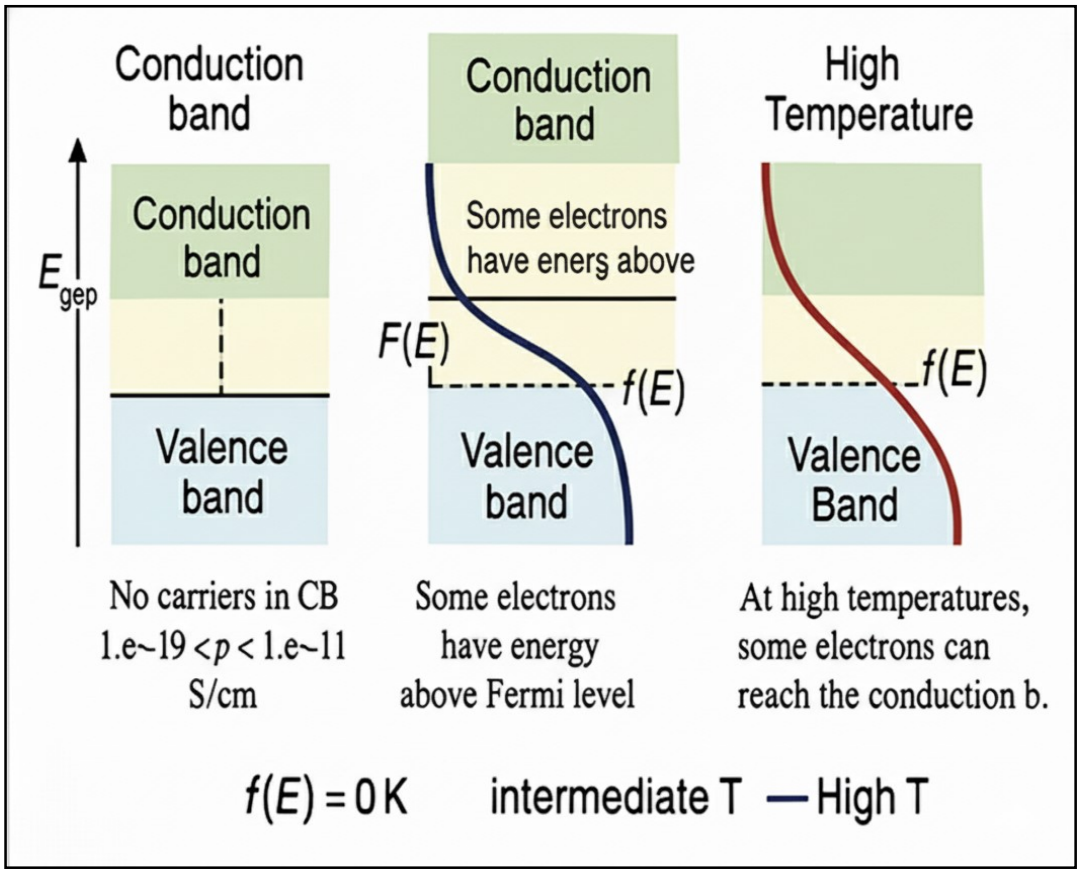


Figure 2.1: Illustration of the implication of the Fermi-Dirac function for the electrical conductivity of a semiconductor.

2.2. Calculation of charge carrier concentrations in the permitted bands

Charge carriers are the free electrons in the conduction band and the free holes in the valence band.

2.2.1. Concentration of free electrons in the conduction band

The concentration of electrons is defined as follows:

$$n = \int_{E_c}^{+\infty} \frac{dn}{dN}.\frac{dN}{dE}.dE = \int_{E_c}^{+\infty} f_n(E).D_c(E).dE \qquad (2.4)$$

$$D_c(E) = \frac{4\pi}{h^3}(2m_n^*)^{\frac{3}{2}}(E - E_c)^{\frac{1}{2}} \qquad (2.5)$$

So :

$$n = \int_{E_c}^{+\infty} \frac{1}{1+\exp\left(\frac{E-E_F}{KT}\right)} \frac{4\pi}{h^3}(2m_n^*)^{\frac{3}{2}}(E - E_c)^{\frac{1}{2}}.dE \qquad (2.6)$$

We make the following approximation: $\boldsymbol{E \gg KT}$

We obtain:

$$n = \frac{4\pi}{h^3}(2m_n^*)^{\frac{3}{2}} \int_{E_c}^{+\infty} \exp\left(\frac{E_F - E}{KT}\right)(E - E_c)^{\frac{1}{2}}.dE \qquad (2.7)$$

We ask:

$A = \frac{4\pi}{h^3}(2m_n^*)^{\frac{3}{2}}$ And $E_F - E = (E_F - E_C) + (E_C - E) = (E_F - E_C) - (E - E_C)$

$$n = A \int_{E_c}^{+\infty} \exp\left[\frac{(E_F - E_C) + (E_C - E)}{KT}\right](E - E_c)^{\frac{1}{2}}.dE \qquad (2.8)$$

$$n = A.\exp\left(\frac{E_F - E_C}{KT}\right) \int_{E_c}^{+\infty} \exp\left(-\left(\frac{E - E_C}{KT}\right)\right).(E - E_c)^{\frac{1}{2}}.dE \qquad (2.9)$$

Posing: $U = \frac{E - E_C}{KT}$; $(E - E_c)^{\frac{1}{2}} = \left(\frac{E - E_c}{kT}\right)^{\frac{1}{2}}.(KT)^{\frac{1}{2}}$

$$n = A.\exp\left(\frac{E_F - E_C}{KT}\right)(KT)^{\frac{1}{2}} \int_{E_c}^{+\infty} \exp(-U).(U)^{\frac{1}{2}}.dU.KT \qquad (2.10)$$

To determine the concentration n we use the following theorems:

$$\begin{cases} \gamma(x) = \int_0^{+\infty} t^{x-1} e^{-t} dt \\ \gamma(x+1) = x\gamma(x) \\ \gamma\left(\frac{1}{2}\right) = \sqrt{\pi} \end{cases} \quad \textbf{(2.11)}$$

We then obtain: $n = \frac{4\pi(KT)^{\frac{3}{2}}}{h^3}(2m_n^*)^{\frac{3}{2}} \exp\left(\frac{E_F - E_C}{KT}\right)$ **(2.12)**

By identification: $x - 1 = \frac{1}{2} \rightarrow x = 1 + \frac{1}{2}$; $\gamma\left(1 + \frac{1}{2}\right) = \frac{1}{2}\gamma\left(\frac{1}{2}\right) = \frac{\sqrt{\pi}}{2}$

$$n = \frac{4\pi}{h^3}(2KTm_n^*)^{\frac{3}{2}} \exp\left(\frac{E_F - E_C}{KT}\right) \quad \textbf{(2.13)}$$

From where ()$\forall\, T°$:

$$n = N_C \exp\left(\frac{E_F - E_C}{KT}\right) \quad \textbf{(2.14)}$$

With: $N_c = \frac{4\pi}{h^3}(2KTm_n^*)^{\frac{3}{2}}$ represents the effective density of state of electrons

2.2.2. Concentration of free holes in the valence band

By the same reasoning we determine the concentration of free holes in the valence band such that ($\forall\, T°$):

$$p = N_V \exp\left(\frac{E_V - E_F}{KT}\right) \quad \textbf{(2.15)}$$

With: $N_V = \frac{4\pi}{h^3}(2KTm_p^*)^{\frac{3}{2}}$ represents the effective state density of holes.

2.3. Classification of semiconductors according to the concentration of charge carriers

2.3.1. Intrinsic semiconductor

An intrinsic semiconductor is a chemically pure semiconductor, i.e., one free of impurities. The number of holes and electrons is determined by the properties of the material itself rather than by impurities. Therefore, in intrinsic semiconductors, the number of excited electrons is equal to the number of holes; n = p.

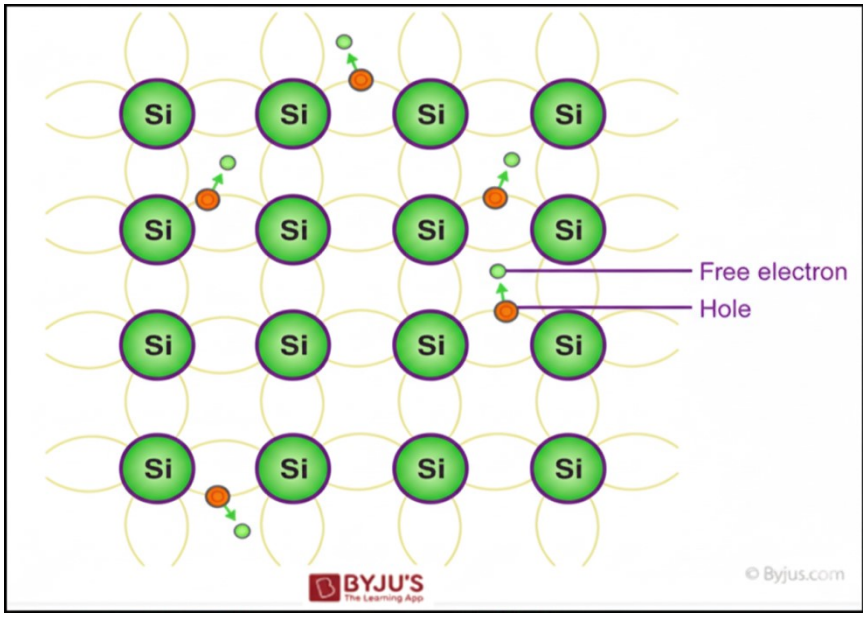


Figure 2.2: Illustration of the intrinsic semiconductors

a. Fermi level

In the case of an intrinsic semiconductor, the concentration of electrons is equal to that of holes.= $p = n_i$

$$N_C \exp\left(\frac{E_{Fi}-E_C}{KT}\right) = N_V \exp\left(\frac{E_V-E_{Fi}}{KT}\right) \quad \textbf{(2.16)}$$

In fact, entering the logarithm on the two terms of the equation gives:

$$\Rightarrow \quad \ln\frac{N_C}{N_V} = \frac{2E_{Fi}-E_g}{KT} \quad \textbf{(2.17)}$$

$$E_{Fi} = \frac{E_C + E_V}{2} - \frac{KT}{2}\ln\frac{N_C}{N_V} \quad (2.18)$$

At 300K N_C and are of the same size N_V:

$$E_{Fi} = \frac{E_C + E_V}{2} \quad (2.19)$$

Noticed: In an intrinsic semiconductor the Fermi level is in the middle of the band gap

b. Calculation of intrinsic concentration

According to the law of mass action:

$$n.p = n_i^2 \quad (2.20)$$

$$N_C \exp\left(\frac{E_{Fi}-E_C}{KT}\right).N_V \exp\left(\frac{E_V-E_{Fi}}{KT}\right) = n_i^2 \quad (2.21)$$

$$n_i = \sqrt{N_C N_V}\exp\left(\frac{-E_g}{2KT}\right) \quad (2.22)$$

2.3.2. Extrinsic semiconductor and temperature effect

It is important to emphasize that in an extrinsic semiconductor the number of charge carriers varies with temperature. There are three distinct temperature regions:

a. Low temperature region: T°<100K

- **Case of an N-type semiconductor**

At low temperatures, intrinsic ionization is very low. Only the electrons in the conduction band prevent thermal ionization of the donors:

If **T°<100K**: $$n_N = \frac{N_D}{1+\exp\left(\frac{E_F-E_D}{KT}\right)} \quad (2.23)$$

If $E_F \gg E_D$: $$n_N = N_D \exp\left(\frac{E_F-E_D}{KT}\right) \quad (2.24)$$

$\forall\, T°$): $$n_N = N_C \exp\left(\frac{E_F - E_C}{KT}\right) \quad (2.25)$$

Therefore: $$n_N = \sqrt{N_C N_D}\exp\left(\frac{E_D - E_C}{2K}\right) \quad (2.26)$$

- **Case of a P-type semiconductor**

If T°<100K $$P_p = \frac{N_A}{1+\exp\left(\frac{E_A - E_F}{KT}\right)} \quad (2.27)$$

If $E_A \gg E_F$: $$P_p = N_A \exp\left(\frac{E_A - E_F}{KT}\right) \quad (2.28)$$

$\forall\, T°$):

$$P_p = N_V \exp\left(\frac{E_V - E_F}{KT}\right) \quad (2.29)$$

So :

$$P_p = \sqrt{N_V N_A}\exp\left(\frac{E_V - E_A}{2KT}\right) \quad (2.30)$$

$(E_D - E_C)$ and represent the ionization energies of the donors and acceptors respectively.$(E_V - E_A)$

b. Medium temperature region: 100K<T°<400K

For intermediate temperatures all impurities are ionized.

- **Case of an N-type semiconductor**

In this case all the donors are ionized, we have: $\mathbf{n_N = N_D}$ **and** $\mathbf{n_N . p_N = n_i^2}$

$$p_N = \frac{n_i^2}{N_D} \quad (2.31)$$

- **Case of a P-type semiconductor**

In this case all the acceptors are ionized, we write: $\mathbf{p_P = N_A}$, $\mathbf{n_P . p_p = n_i^2}$

→ $$n_P = \frac{n_i^2}{N_A} \quad (2.32)$$

c. High temperature region T°>400K

In this temperature range the extrinsic semiconductor behaves like an intrinsic semiconductor, therefore: and $\mathbf{n_P = p_p = n_i}$ **and** $\mathbf{n_N = p_N = n_i}$

2.4. Determination of the Fermi level

It is very important to know the position of the Fermi level E_F since it determines the concentrations of free carriers. Also, knowing its position allows us to know the electronic transport properties (conductivity, etc.) in semiconductors. To determine the position and energy $E_F$of the Fermi level, taking the case of an extrinsic semiconductor with N_D donor andN_A acceptors. will be deduced after solving the neutrality equation

$$n + N_A^- = p + N_D^+ \quad \textbf{(2.33)}$$

With n and p, being the respective concentrations of electrons and holes. And N_D^+ , N_A^-represent the concentrations of the ionized donor and acceptor dopants respectively.

$$\begin{cases} N_D = N_D^+ + N_D^0 \\ N_A = N_A^- + N_A^0 \end{cases} \quad \textbf{(2.34)}$$

$N_D\ et\ N_A$are the total concentrations of donors and acceptors respectively. $N_D^0\ and\ N_A^0$ are the concentrations of non-ionized donors and acceptors respectively.

$$N_D = \frac{N_D^+}{1 + \exp\left(\frac{E_F - E_D}{KT}\right)} \quad \textbf{(2.35)}$$

$$N_A = \frac{N_A^-}{1 + \exp\left(\frac{E_A - E_F}{KT}\right)} \quad \textbf{(2.36)}$$

2.4.1. Approximate method

a. Low temperature region

- **Case of an N-type semiconductor**

$$n = N_C \exp\left(\frac{E_F - E_C}{KT}\right) = \mathrm{N_D}\exp\left(\frac{\mathrm{E_D - E_{FN}}}{\mathrm{KT}}\right) \quad (2.37)$$

$$\mathrm{E_{FN}} = \frac{E_C + E_D}{2} + \frac{KT}{2}\ln\frac{N_D}{\mathrm{N_C}} \quad (2.38)$$

- **P-type semiconductor**

$$p = N_V \exp\left(\frac{E_V - E_F}{KT}\right) = \mathrm{N_A}\exp\left(\frac{\mathrm{E_{FP} - E_A}}{\mathrm{KT}}\right) \quad (2.39)$$

$$\mathrm{E_{FP}} = \frac{E_V + E_A}{2} - \frac{KT}{2}\ln\frac{N_A}{\mathrm{N_V}} \quad (2.40)$$

b. Intermediate temperature region

- **N-Type Semiconductor**

In this case:

$$n = N_C \exp\left(\frac{E_F - E_C}{KT}\right) = \mathrm{N_D} \quad (2.41)$$

$$\mathrm{E_{FN}} = E_C + KT\ln\frac{N_D}{\mathrm{N_C}} \quad (2.42)$$

- **P-Type Semiconductor**

In this case: $$p = N_V \exp\left(\frac{E_V - E_F}{KT}\right) = \mathrm{N_A} \quad (2.43$$

$$\mathrm{E_{FP}} = E_V - KT\ln\frac{N_A}{\mathrm{N_V}} \quad (2.44)$$

c. High temperature region

In this region, the extrinsic semiconductor (N or P) behaves like an intrinsic semiconductor such that:

$$E_{Fi} = \frac{E_C + E_V}{2} - \frac{KT}{2} \ln \frac{N_C}{N_V}$$

2.4.2. Graphical method

Based on the neutrality equation, the Fermi level can be determined graphically as follows:

$$n + N_A^- = p + N_D^+ \quad \textbf{(2.45)}$$

We entered the natural logarithm on both sides of the equation, we obtain

$$\ln(n + N_A^-) = \ln(p + N_D^+) \quad \textbf{(2.46)}$$

a. Let's draw first $\ln(n)$

We have:

$$n = N_C \exp\left(\frac{E_F - E_C}{KT}\right) \quad \textbf{(2.47)}$$

$$\ln(n) = \ln(N_C) + \frac{E_F - E_C}{KT} \quad \textbf{(2.48)}$$

If $E_F = E_C$ >>>>>>>> $\ln(n) = \ln(N_C)$

If >>>>>>>>>$E_F = E_V$ $\ln(n) = \ln(N_C) + \frac{E_V - E_C}{KT} = \ln(N_C) - \frac{E_g}{KT}$ **(2.49)**

b. Let's draw $\ln(p)$

$$p = N_V \exp\left(\frac{E_V - E_F}{KT}\right) \quad \textbf{(2.50)}$$

$$\ln(p) = \ln(N_V) + \frac{E_V - E_F}{KT} \quad \textbf{(2.51)}$$

If $E_F = E_V$ >>>>> $\ln(p) = \ln(N_V)$

If $E_F = E_C$ >>>>>>>> $\ln(p) = \ln(N_V) + \frac{E_V - E_C}{KT} = \ln(N_V) - \frac{E_g}{KT}$ **(2.52)**

c. Let's draw $\ln(N_D^+)$ *et* $\ln(N_A^-)$

For N_D^+ : $$N_D^+ = \frac{N_D}{1+\exp\left(\frac{E_F-E_D}{KT}\right)} \quad \textbf{(2.53)}$$

If $E_F > E_D$ >>>>>>>> $\ln(N_D^+) = \ln(N_D) + \frac{E_D-E_F}{KT}$ **(2.54)**

- If $E_F = E_D$ >>>>>>>> $\ln(N_D^+) = \ln(N_D)$ **(2.55)**
- If $E_F = E_C$ >>>>>>>> $\ln(N_D^+) = \ln(N_D) + \frac{E_D-E_C}{KT}$ **(2.56)**
- If $E_F < E_D$ >>>>>>>> $\ln(N_D^+) = \ln(N_D)$ **(2.57)**

For N_A^- : $$N_A^- = \frac{N_A}{1+\exp\left(\frac{E_A-E_F}{KT}\right)} \quad \textbf{(2.58)}$$

If $E_F > E_A$ >>>>>>>> $\ln(N_A^-) = \ln(N_A) + \frac{E_F-E_A}{KT}$ **(2.59)**

- If $E_F = E_A$ >>>>>>>> $\ln(N_A^-) = \ln(N_A)$ **(2.60)**
- If $E_F = E_V$ >>>>>>>> $\ln(N_A^-) = \ln(N_A) + \frac{E_V-E_A}{KT}$ **(2.61)**
- If $E_F < E_D$ >>>>>>>> $\ln(N_A^-) = \ln(N_A)$ **(2.62)**

Approximation:

To plot $\ln(n + N_A^-)$ we make the following approximation:

If $n > N_A^-$ >>>>>>>> $\ln(n + N_A^-) = \ln(n)$ **(2.63)**

If $n < N_A^-$ >>>>>>>> $\ln(n + N_A^-)\ln(N_A^-)$ **(2.64)**

To plot $\ln(p + N_D^+)$ we make the following approximation:

If $p > N_D^+$ >>>>>>>> $\ln(p + N_D^+) = \ln(p)$ **(2.65)**

If $p < N_D^+$ >>>>>>>> $\ln(p + N_D^+)\ln(N_D^+)$ **(2.66)**

We determine graphically $\ln(n + N_A^-)$ and $\ln(p + N_D^+)$ as a function of E_F, the intersection of the two curves determines the position of at a given temperature. By simply reading the graph we can deduce.$E_F, n,\ N_A^-;\ p\ and\ N_D^+$

Note: In all calculations the temperature is fixed.

2.5. Electronic transport principle

2.5.1 Study of charge transport mechanisms

For an intrinsic semiconductor **$n=p=n_i$**. When the crystal is not subjected to any external excitation, it is in equilibrium. At 0°C, all electrons are in the valence band. In this case, the semiconductor behaves like an insulator (the charges are immobile). Under the effect of a temperature gradient, energy is transmitted to the crystal; certain electrons can pass from the valence band (BV) to the conduction band (BC), crossing the band gap (BI). To be able to carry out this movement, the electrons must have an energy ≥ the gap Eg. The released electrons acquire certain energy; translated by a thermal velocity ϑ. The electrons follow random paths with the atoms in the lattice.

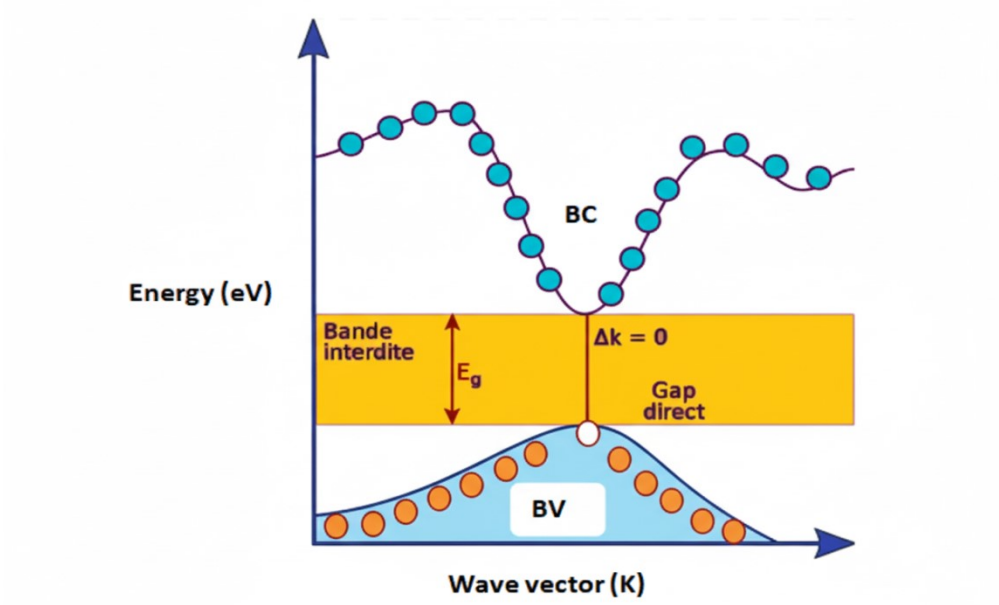


Figure 2.3: Representation of a direct bandgap semiconductor

The momentum of the electrons is then: $m_n^*.\vartheta = \hbar k$ **(2.67)**

With: the effective mass of the electrons and the wave vector. $m_n^*\ k$ **(2.68)**

The average speed of electrons is calculated by: $\frac{1}{2}m_n^*\bar{\vartheta}^2 = \frac{3}{2}KT$ **(2.69)**

K: Boltzmann constant, $\bar{\vartheta}$: average speed

The mean free path can be defined as the average distance traveled between two collisions, to which we associate an average time called such that:$\bar{l}\tau\bar{l} = \tau.\bar{\vartheta}$

2.5.2 Applying an electric field to the crystal

a. Mobility of electrons and holes

By applying an electric field $\vec{E}$ to the crystal, the electrons are subjected to an electric force$\vec{F}$ given by: $\vec{F} = m_n^*.\frac{dv_n}{dt} = -q\vec{E}$ **(2.70)**

If at t=0,$v_n = v_0 \gg\gg\gg\gg\gg \frac{\mathrm{dv_n}}{\mathrm{dt}} = -\frac{\mathrm{qE}}{\mathrm{m_n^*}} \gg\gg\gg\gg\gg v_n - v_0 = -\frac{qEt}{m_n^*}$ **(2.71)**

If at t= τ, v_n=$\bar{\vartheta} \gg\gg\gg\gg\gg \bar{\vartheta} - v_0 = -\frac{q\tau}{m_n^*} E = \mu_n E$ or μ_n represents the mobility of the electrons: $|\mu_n| = \frac{V}{E} = \frac{q\tau}{m_n^*}\left(\frac{cm^2}{V.s}\right)$ **(2.72)**

A similar reasoning allows us to define the mobility of holes

$$|\mu_p| = \frac{V}{E} = \frac{q\tau}{m_p^*}\left(\frac{cm^2}{V.s}\right) \quad \textbf{(2.73)}$$

Noticed: Generally $\boldsymbol{\mu_n \approx 3\mu_p}$

b. Electrical conductivity

Let and be the volume densities of charges of electrons and holes respectively. The densities of conduction currents are respectively:ρ_n ρ_p

$$\overrightarrow{J_n^c} = \rho_n\overrightarrow{\vartheta_n^c}, \overrightarrow{J_p^c} = \rho_p\overrightarrow{\vartheta_p^c} \quad \textbf{(2.74)}$$

$$\overrightarrow{\vartheta_n^c} = -\mu_n.\vec{E}\ , \overrightarrow{\vartheta_p^c} = \mu_p.\vec{E} \quad \textbf{(2.75)}$$

$$\overrightarrow{J_n^c} = -\rho_n\mu_n.\vec{E}\overrightarrow{J_p^c} = \rho_p\mu_p.\vec{E} \quad \textbf{(2.76)}$$

with $\rho_n = -qn\ \ and\ \ \rho_p = qp$, $\overrightarrow{J_n^c} = qn\mu_n.\vec{E}$ and $\overrightarrow{J_p^c} = qp\mu_p.\vec{E}$

Subsequently $\overrightarrow{J_n^c} = \sigma_n.\vec{E}$ and $\overrightarrow{J_p^c} = \sigma_p.\vec{E}$

$\sigma_n = qn\mu_n$ and $\sigma_p = qn\mu_p$ are respectively the electrical conductivities of electrons and holes expressed in $\Omega^{-1}cm^{-1}$

The total current density is therefore:

$$\overrightarrow{J_{tot}^c} = \overrightarrow{J_n^c} + \overrightarrow{J_p^c} = q(n\mu_n + p\mu_p)\vec{E} \quad \textbf{(2.77)}$$

Where $\sigma_{tot} = q(n\mu_n + p\mu_p)$

If the semiconductor is intrinsic $n = p = n_i$

$\sigma_{tot} = qn_i(\mu_n + \mu_p)$ and $\rho_{tot} = \frac{1}{\sigma_{tot}} = \frac{1}{(qn_i(\mu_n+\mu_p)}$

If the semiconductor is N-type, the concentration of electrons increases.

At 300K ⇨ $n = N_D\overrightarrow{J_{tot}^c} = \overrightarrow{J_n^c} = qN_D\mu_n\vec{E}$ **(2.78)**

If the semiconductor is P-type, the concentration of holes increases.

At 300K. ⇨ $p = N_A\overrightarrow{J_{tot}^c} = \overrightarrow{J_p^c} = qN_A\mu_p\vec{E}$ **(2.79)**

2.5.3 Diffusion and continuity equations of minority carriers

a. Diffusion of minority interests

In a semiconductor, the movement of free carriers is due either to entrainment under the effect of an applied electric field, or to diffusion when there is a concentration gradient. When the semiconductor is subjected to light excitation, i.e. photonic energy ($E = h\upsilon = \frac{\hbar C}{\lambda}$), excess charge carriers are created in the illuminated region compared to the equilibrium concentrations $\bar{n}\ and\ \bar{p}$. We therefore have a non-equilibrium phenomenon due to the increase in concentrations n and p

For an N-type semiconductor at equilibrium $\bar{n} = N_D$, and if the semiconductor is P-type. $\bar{p} = N_A$

We will study the diffusion of minority carriers in the case of a P-type semiconductor ($\bar{p} > \bar{n}$).

Note that diffusion only concerns minority carriers, which in this case are electrons. These are more numerous in the illuminated medium and move towards the low concentration region.

Minority carriers move from the region of higher concentration to the region of lower concentration in order to achieve a uniform charge balance

The medium after excitation must become electrically neutral. The electrons will recombine with the holes and it is only at a certain distance from the illuminated region that the equilibrium concentration is found. We say that diffusion of minority carriers occurs each time there is a concentration gradient and it tends to flow in the direction of decreasing concentrations.$\bar{n}$.

The flow of electrons is expressed by: $F_n = -D_n \overrightarrow{grad} n = -\frac{dn}{dx}$ **(2.80)**

In the case of an N-type semiconductor: $F_p = -D_p \overrightarrow{grad} P = -\frac{dp}{dx}$ **(2.81)**

$D_n \; et \; D_p$ are the diffusion constants of electrons and holes respectively

We deduce the diffusion currents:

For electrons: $\overrightarrow{J_n^D} = -q\vec{F}_n = qD_n \overrightarrow{grad} n = qD_n \frac{dn}{dx}$ **(2.82)**

For the holes: $\overrightarrow{J_p^D} = -q\vec{F}_p = qD_p \overrightarrow{grad} P = qD_p \frac{dp}{dx}$ **(2.83)**

A semiconductor contains both types of charge carriers. These carriers move under the effect of:

- An electric field: we therefore have a conduction current
- A concentration gradient: we therefore have a conduction current

In the case of a semiconductor where the concentration of carriers is not uniform and to which an electric field is applied, we will therefore have the sum of the two diffusion and conduction currents: $J_{tot} = J^c + J^D$

So: $$J_n = J_n^D + J_n^c = qD_n\overrightarrow{grad}n + qn\mu_n.\vec{E} \quad \textbf{(2.84)}$$

$$J_p = J_p^D + J_p^c = qD_p\overrightarrow{grad}P + qp\mu_p.\vec{E} \quad \textbf{(2.85)}$$

Noticed: At thermodynamic equilibrium the total current densities are zero

b. Einstein's relationships

They are expressed as follows: $$\frac{D_n}{\mu_n} = \frac{D_p}{\mu_p} = \frac{KT}{q} \quad \textbf{(2.86)}$$

c. Non-equilibrium semiconductor (injection and extraction of charge carriers)

Most electronic devices operate outside of equilibrium conditions. At thermodynamic equilibrium: $\bar{n}.\bar{p} = n_i^2$

In the non-equilibrium case $n.p \neq n_i^2$, where n *and* p are the non-equilibrium concentrations of electrons and holes.

If $n.p > n_i$: we are talking about carrier injection

If $n.p < n_i$: we are talking about carrier extraction

$$\begin{cases} n = \bar{n} + D_n = n + \hat{n} \\ p = \bar{p} + D_p = p + \hat{p} \end{cases} \quad \textbf{(2.87)}$$

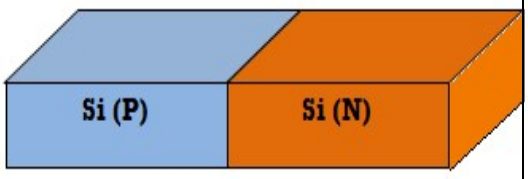
$\hat{n}$ *et* $\hat{p}$: are the concentrations of excess electrons and holes.

Chapter III: PN Junction physic

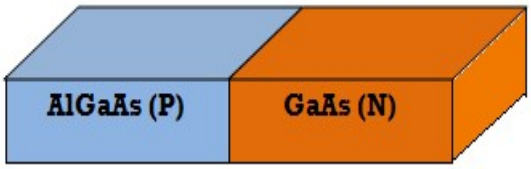
Introduction

The PN junction plays an important role in current electronics. It is involved in the production of many electronic devices and circuits, including diodes, bipolar transistors, JFET field-effect transistors, and solar cells. The PN junction is obtained by juxtaposing two differently doped P and N semiconductors. It is not just a simple juxtaposition of two semiconductors; the contact between the two semiconductors must be a continuity of the crystal lattice on either side of the junction surface.

There are two types of junctions:

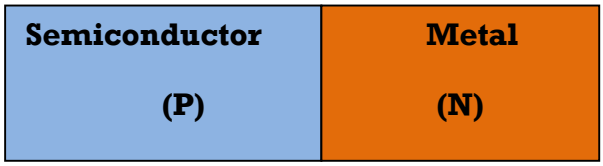


a. **Homojunction**: we speak of Homojunction when the junction is obtained from a single semiconductor bar such as silicon or germanium.



b. **Heterojunction:** the heterojunction is made from two different semiconductors

If the semiconductor type is replaced by a conductor (metal) the junction is called: Schottky junction



The doping of both N and P regions is done either by the diffusion process or by ion implantation (for more details on these two processes, see the course "**integrated circuit manufacturing technology**").

Depending on the evolution of the concentration of dopants, two types of homojunction are distinguished:

- **Abrupt homojunction**:

The junction is said to be abrupt when the NA and ND concentrations are constant across the semiconductor rod. Otherwise, an abrupt junction is by definition a junction in which the doping type changes over a very small distance compared to the spatial extent of the depletion region.

- **Gradual homojunction**:

In this type of junction the NA and ND concentrations vary gradually.

In this chapter, a simplified one-dimensional (1D) qualitative study of the properties of a Homojunction will be presented.

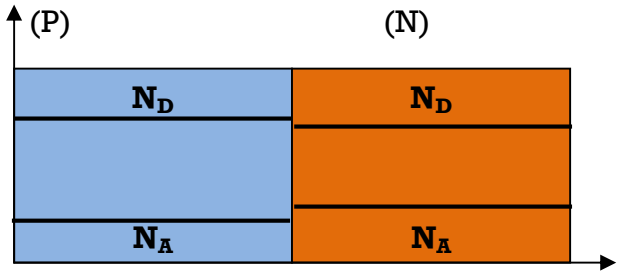


Figure 3.1: Abrupt homojunction

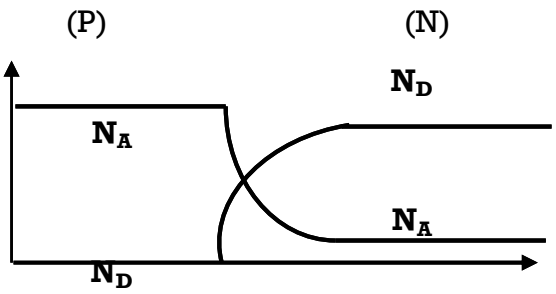


Figure 3.2: Gradual homojunction

3.1 Qualitative study of the operation of a junction

We place ourselves at an ordinary temperature of 300K without any external disturbance. We create an abrupt junction by gradually bringing together two crystals with different doping. Before physical contact between the two regions, there is equilibrium and all the dopants are ionized.

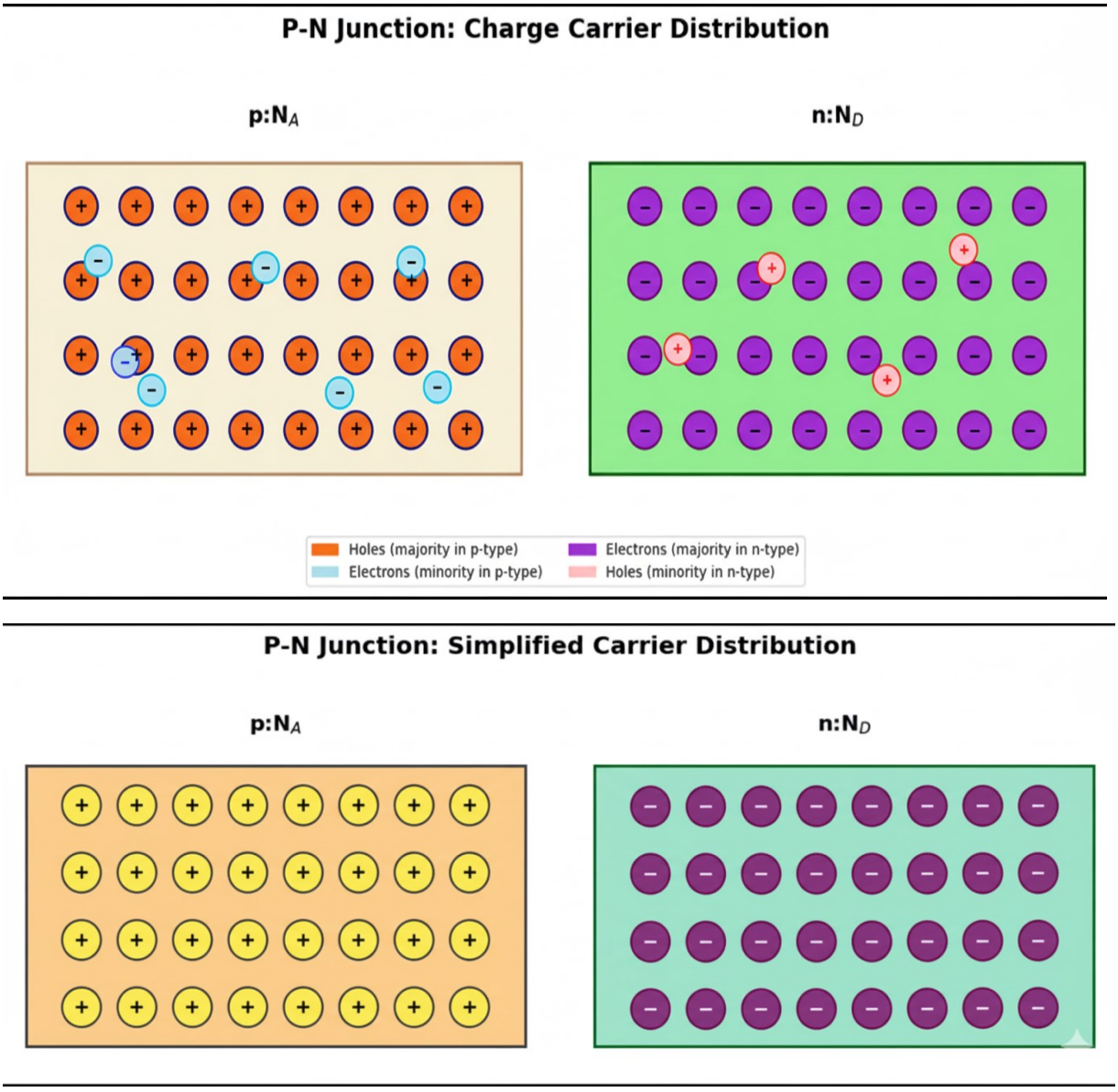


Figure 3.3: P-N Junction diagram with charge carriers

When contact is established, a concentration gradient appears on either side of the contact surface. The carriers diffuse from the more doped side to the less doped side (see figure below). We therefore have:

- An electron flow towards the P region
- A flow of holes to the N region

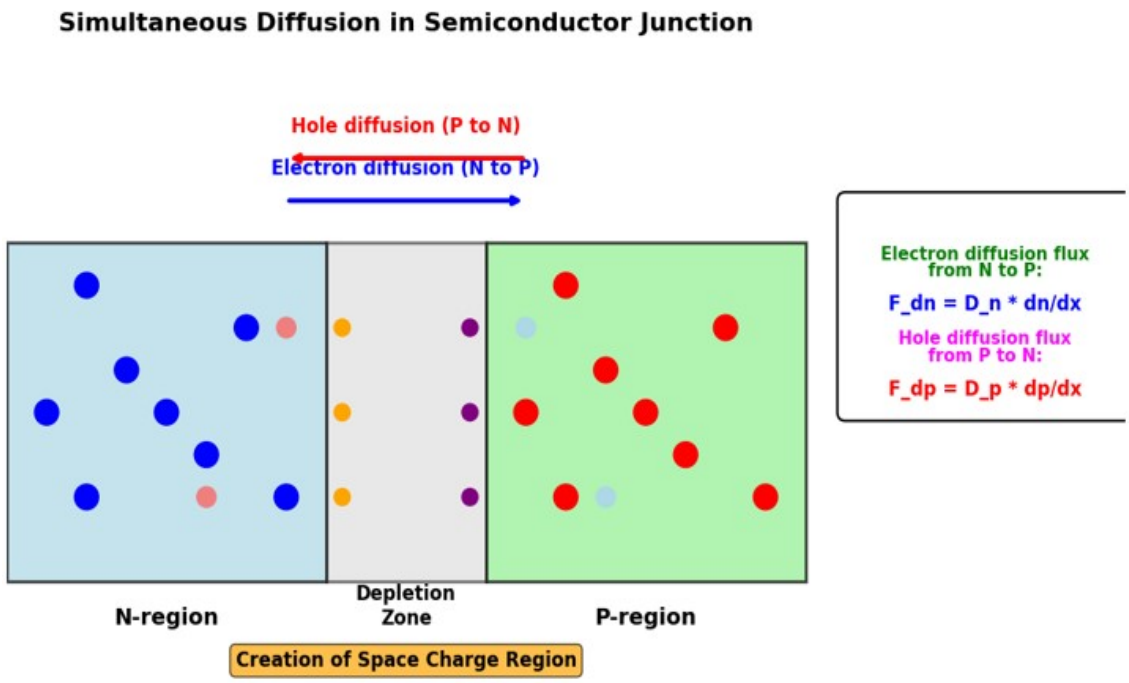


Figure 3.4: Simultaneous diffusion in PN Junction

When equilibrium is established, a depleted area (depletion region) of charges is formed. This area is called the space charge zone SCZ. In this area, an internal electric field called "diffusion field" is produced. It is directed from the N side (positively charged) to the P side (negatively charged).

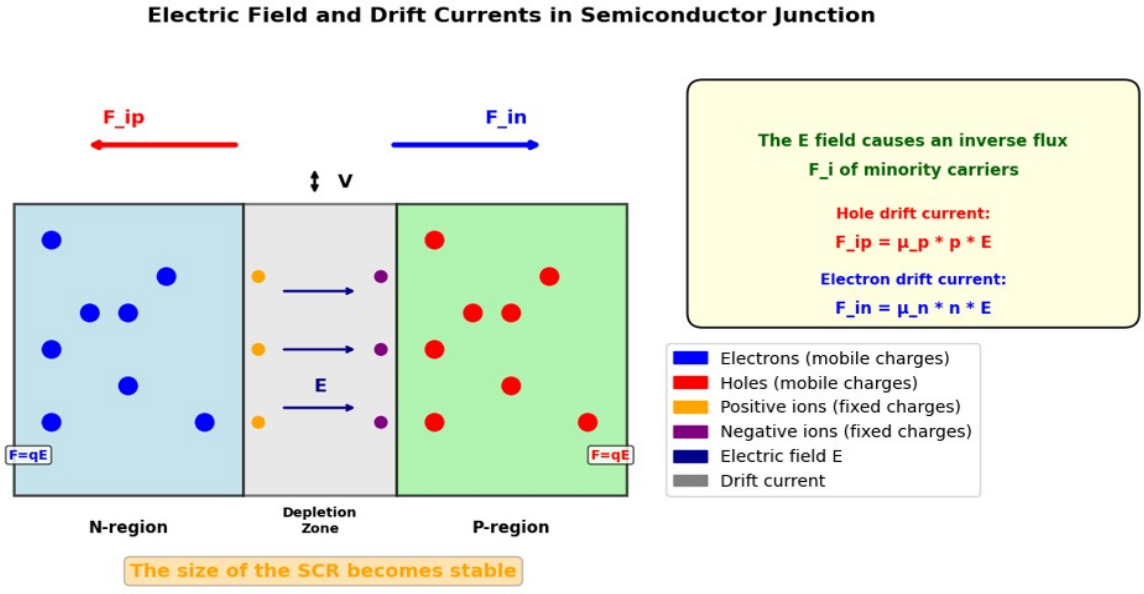


Figure 3.5: Representation of the internal electric field in the SCZ.

When the diffusion field becomes strong enough it opposes the diffusion phenomenon of the majority until thermodynamic equilibrium has occurred and diffusion is composed by conduction (J_N=J_P=0). Moreover, at thermodynamic equilibrium, diffusion and internal fluxes become equal i.e., F_{in}=F_{dn} **(N side)** and **F_{ip}=F_{dp} (P side).** In this case the Fermi level remains constant throughout the structure.

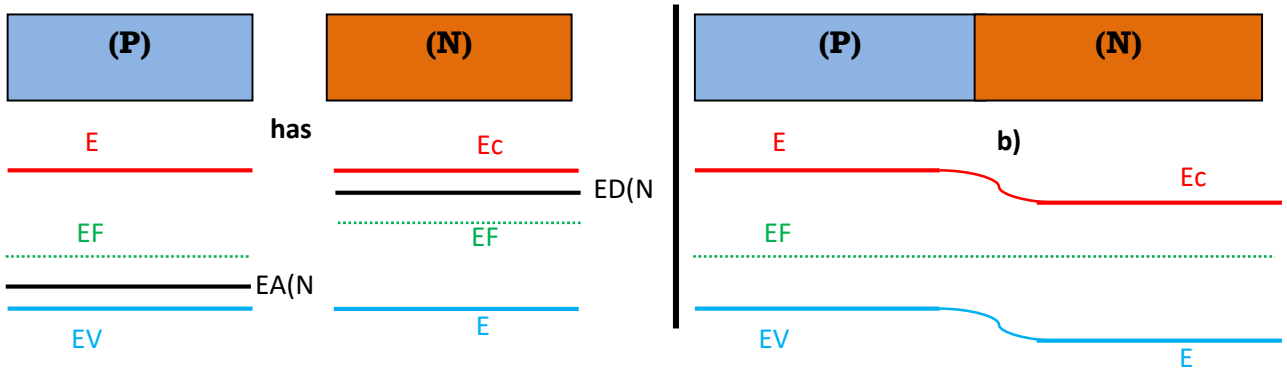


Figure 3.6: Representation of the Fermi level:

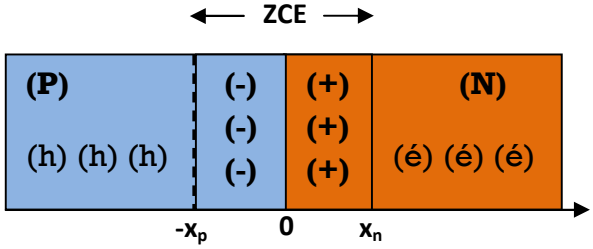
Left) Before junction contact; **Right)** After contact.

3.2 Study of the abrupt PN junction

3.2.1. Charges distribution

The equation that describes the charge density ρ(x) across the depletion region is given by:

$$\rho(x) = \begin{cases} +qN_D & si \;\; 0 < x < x_n \\ -qN_A & si \;\; -x_p < x < 0 \\ 0 & ailleurs \end{cases} \qquad (3.1)$$



So, the charge is not uniform; it's a dipole layer of fixed opposite charges on either side of the junction.

3.2.2. Variation of the electric field

To determine the spatial distribution of the electric field across the junction we used Poisson's equation:

$$divE = \frac{\rho(x)}{\varepsilon} \gg\gg\gg\gg\gg\gg\gg\gg \frac{dE}{dx} = \frac{\rho(x)}{\varepsilon} \quad (3.2)$$

With: $\varepsilon = \varepsilon_0 + \varepsilon_r$

If $0 < x < x_n$:

$$\frac{dE}{dx} = \frac{+qN_D}{\varepsilon} \gg\gg\gg\gg\gg E_n(x) = \int \frac{+qN_D}{\varepsilon} dx \quad (3.3)$$

$$E_n(x) = \frac{+qN_D}{\varepsilon} x + cst1 \quad (3.4)$$

To determine the constant cst1 we use the boundary condition:

$$x = x_n \gg\gg\gg\gg\gg\gg E_n(x_n) = 0 \gg\gg\gg\gg\gg\gg cst1 = \frac{-qN_D x_n}{\varepsilon} \quad (3.5)$$

So:

$$E_n(x) = \frac{qN_D}{\varepsilon} x - \frac{qN_D}{\varepsilon} x_n = \frac{qN_D}{\varepsilon}(x - x_n) \quad (3.6)$$

If $-x_p < x < 0$:

$$\frac{dE}{dx} = \frac{-qN_A}{\varepsilon} \gg\gg\gg\gg E_p(x) - \int \frac{qN_A}{\varepsilon} dx \quad (3.7)$$

$$E_p(x) = \frac{-qN_A}{\varepsilon} x + cst2 \quad (3.8)$$

In the same way we determine the cst2:

$$x = -x_p \gg\gg\gg\gg\gg\gg E_p(-x_p) = 0 \gg\gg\gg\gg\gg\gg cst1 = -\frac{qN_A x_p}{\varepsilon} \quad (3.9)$$

So:

$$E_p(x) = -\frac{qN_A}{\varepsilon} x + \frac{qN_A}{\varepsilon} x_p = -\frac{qN_A}{\varepsilon}(x + x_p) \quad (3.10)$$

According to the condition of continuity of the electric field $E_n(x = 0) = E_p(x = 0)$:

$$x_n N_D = x_p N_A$$

From this last equation we conclude that the SCZ extends on the weakly doped side.

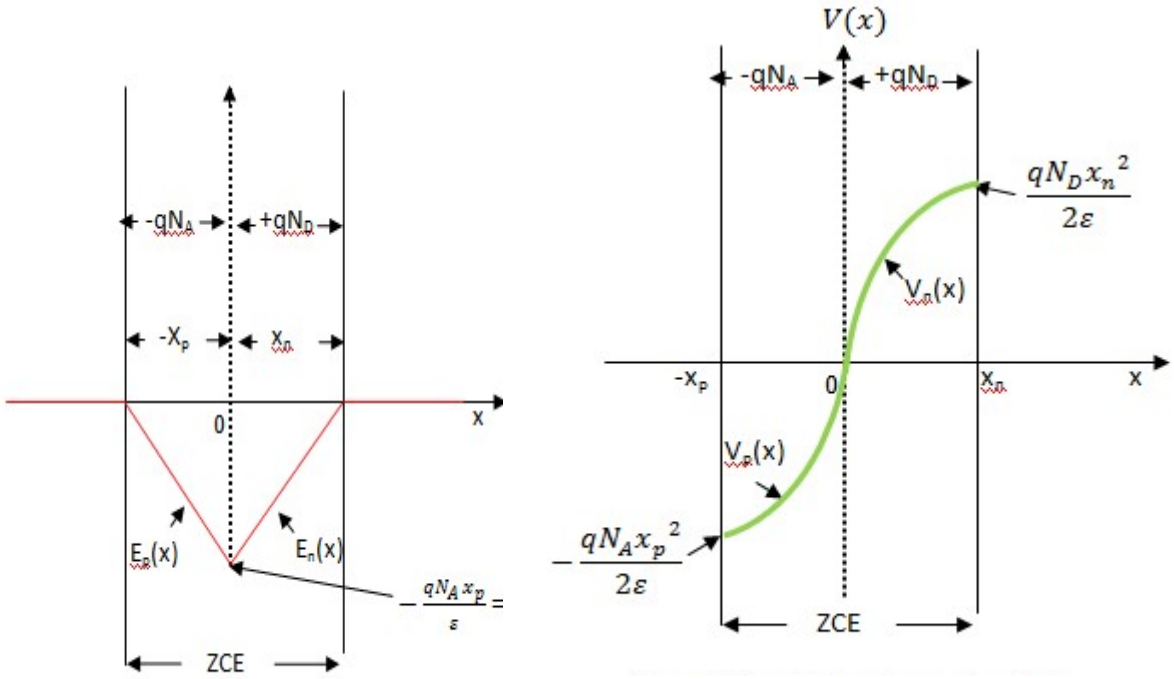


Figure 3.7: Distribution across the depletion region of: **Left**: Electric field, **Right**: Electrostatic potential

3.2.3. Distribution of electrostatic potential

If $0 < x < x_n$:

$$E = -grad\, V \quad \gg\gg\gg\gg V = -\int E dx \tag{3.11}$$

$$V_n(x) = -\frac{qN_D}{\varepsilon}\int (x - x_n)dx \tag{3.12}$$

$$V_n(x) = -\frac{qN_D}{2\varepsilon}(x^2 - 2xx_n) + cst1 \tag{3.13}$$

If $-x_p < x < 0$:

$$V_p(x) = \frac{qN_A}{\varepsilon}\left(x^2 + xx_p\right) + cst2 \tag{3.14}$$

We admit that there is continuity in $x = 0$,

$$V_n(x = 0) = V_p(x = 0) = 0 \gg cst1 = cst2 = 0 \tag{3.15}$$

So: $$V_n(x) = -\frac{qN_D}{2\varepsilon}(x^2 - 2xx_n) \tag{3.16}$$

$$V_p(x) = \frac{qN_A}{2\varepsilon}\left(x^2 + 2xx_p\right) \quad \textbf{(3.17)}$$

3. 2.4. Diffusion voltage

The potential difference in the PN junction is expressed by:V_D

$$V_D = V_n(x_n) - V_p(-x_p) = \frac{q}{2\varepsilon}(N_D {x_n}^2 + N_A {x_p}^2) \quad \textbf{(3.18)}$$

We deduce: $$V_D = \frac{KT}{q}\ln\left(\frac{N_A N_D}{{n_i}^2}\right) \quad \textbf{(3.19)}$$

$$ {n_i}^2 = N_C N_V \ \exp\left(\frac{-E_g}{KT}\right) \quad \textbf{(3.20)}$$

3.2.5. Calculation of the width of the SCZ: W_{SCZ}

$$x_n = \sqrt{\frac{2\varepsilon V_D N_A}{qN_D(N_A + N_D)}} \quad \textbf{(3.21)}$$

$$x_p = \sqrt{\frac{2\varepsilon V_D N_D}{qN_A(N_A + N_D)}} \quad \textbf{(3.22)}$$

$$W_{SCZ} = x_n + x_p = \sqrt{\frac{2\varepsilon V_D}{q}\frac{N_{A+}N_D}{(N_A N_D)}} \quad \textbf{(3.23)}$$

3.2.6. Diffusion capacity: C_d

We assume that SCZ is a thick insulator surrounded by two slightly conductive regions. So we have the structure of a planar capacitor. Its capacitance is called diffusion capacitance and is noted C_d as follows:

$$C_d = \frac{\varepsilon S}{W_{SCZ}} = S\sqrt{\frac{q\varepsilon}{2}\frac{N_A N_D}{V_D(N_A + N_D)}} \quad \textbf{(3.24)}$$

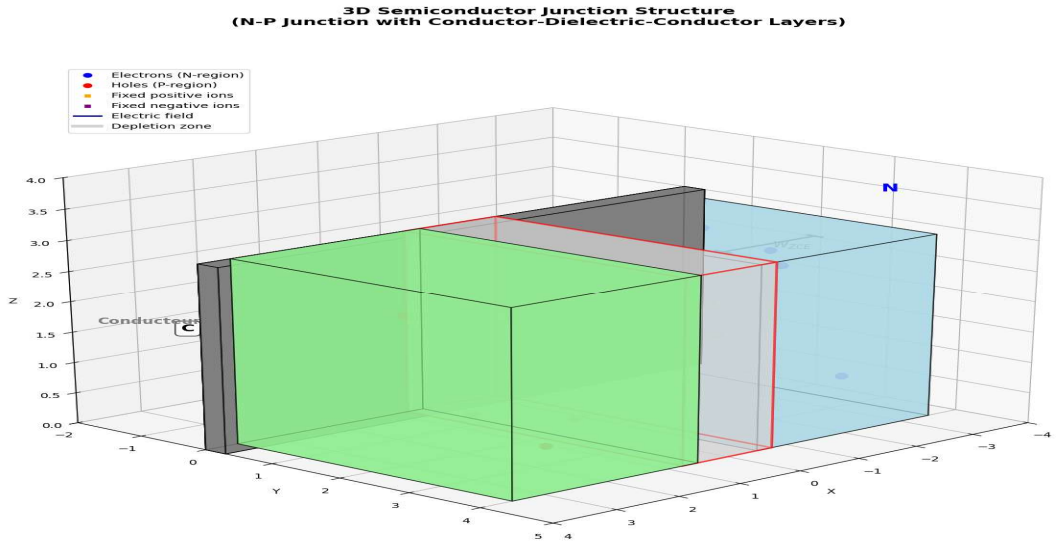


Figure 3.8: Illustration of the junction capacity

3.3 Polarization of the PN junction

We speak of a polarized junction when its terminals are connected to an external voltage generator V. It's aims to create an electric field to drain the electrons in order to generate an electric current in the junction. By convention, the current of the junction is positive when it flows from the P region to the N region. Two modes of polarization are distinguished:

3.3.1 Forward polarization

The voltage across the junction will therefore be: $U = V_D - V$. Subsequently, the width of the depletion region, as well as the diffusion capacity become respectively:

$$W_{ZCE} = x_n + x_p = \sqrt{\frac{2\varepsilon(V_D - V)}{q}\frac{N_{A+}N_D}{(N_A N_D)}} \quad (3.25)$$

$$C_d = \frac{\varepsilon S}{W_{ZCE}} = S\sqrt{\frac{q\varepsilon}{2(V_D - V)}\frac{N_A N_D}{(N_A + N_D)}} \quad (3.26)$$

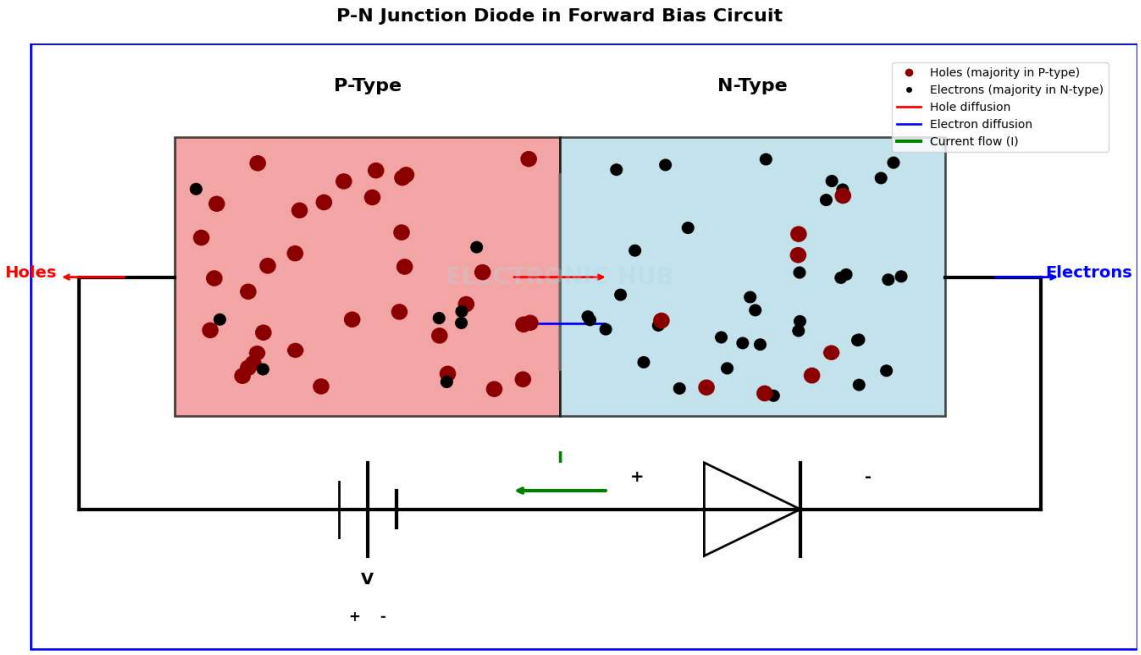


Figure 3.9: Forward biased PN junction

3.3.2 Reverse bias

In this case the voltage across the junction will therefore be: $U = V_D + V$. In this case, the width of the depletion region, as well as the diffusion capacity are expressed as follow:

$$W_{ZCE} = x_n + x_p = \sqrt{\frac{2\varepsilon(V_D + V)}{q}\frac{N_{A+}N_D}{(N_A N_D)}} \quad (3.27)$$

$$C_d = \frac{\varepsilon S}{W_{ZCE}} = S\sqrt{\frac{q\varepsilon}{2(V_D + V)}\frac{N_A N_D}{(N_A + N_D)}} \quad (3.28)$$

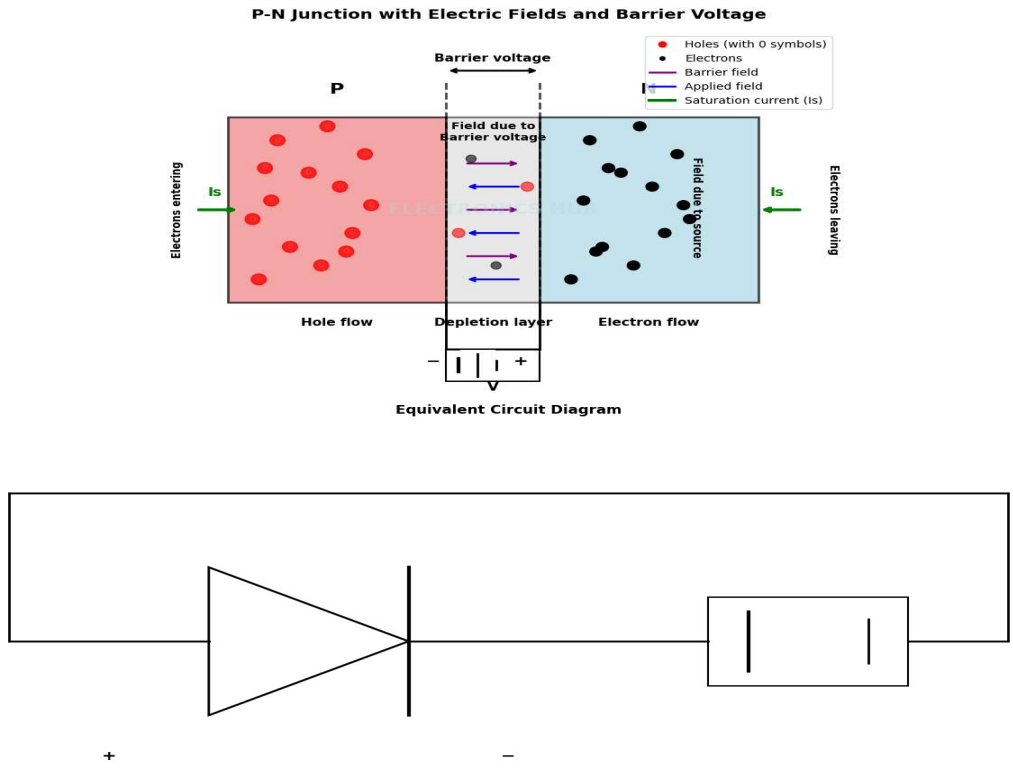


Figure 3.10: Reverse biased PN junction

3.4 Concentration of charge carriers within the boundaries of the PN junction

Based on the equation: $np = n_i^2$, the distribution of charge carriers, majority and minority, across the junction is given in the figure 3.11.

In balance:

$$P_p = \overline{P_p} = N_A \quad \text{and} \quad n_n = \overline{n_n} = N_D$$

$$n_p = \overline{n_p} e^{\frac{qv}{KT}} \quad \text{and} \quad P_n = \overline{p_n} e^{\frac{qv}{KT}}$$

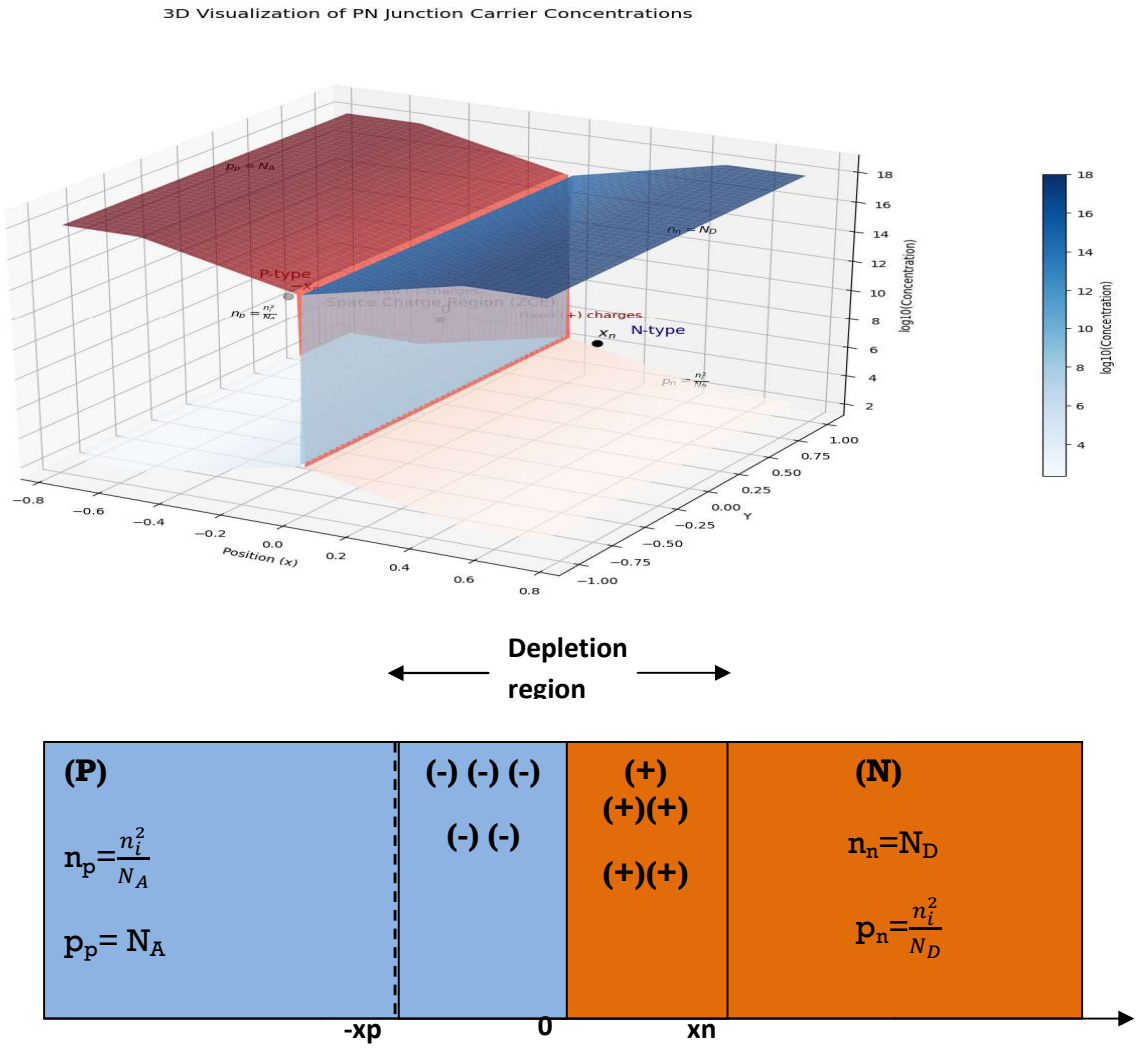


Figure 3.11: Visualization of PN junction carrier's concentration

3.5 Spatial distribution of currents at the junction

The current across a p–n junction originates from the diffusion of minority carriers injected into the quasi-neutral regions under bias. Holes from the p-side diffuse into the n-side, while electrons from the n-side diffuse into the p-side. These contributions can be described mathematically as position-dependent diffusion currents, expressed in terms of carrier diffusion lengths, equilibrium minority concentrations, and the applied voltage.

$$I_p(x) = -\frac{qSD_p}{L_p}\overline{p_n}[exp^{\frac{qv}{KT}} - 1]exp^{\frac{x_n - x}{L_p}} \quad \textbf{(3.29)}$$

$$I_n(x) = -\frac{qSD_n}{L_n}\overline{n_p}[exp^{\frac{qv}{KT}} - 1]exp^{\frac{x_p+x}{L_n}} \quad \textbf{(3.30)}$$

$$I(x) = qS[\frac{D_n}{L_n}\overline{n_p} + \frac{D_p}{L_p}\overline{p_n}](exp^{\frac{qv}{KT}} - 1) = I_s(exp^{\frac{qv}{KT}} - 1) \quad \textbf{(3.31)}$$

With: S represents the surface of the junction, D_n *and* D_p are respectively the diffusion constants of electrons and holes. L_n ; L_p are respectively the diffusion lengths of electrons and holes. I_s represents the saturation current of the diode and is expressed as follow:

$$I_s = qS[\frac{D_n}{L_n}\overline{n_p} + \frac{D_p}{L_p}\overline{p_n}] \quad \textbf{(3.32)}$$

3.6 Junction breakdown

By applying a reverse voltage greater than a certain critical value across the junction, the reverse current increases rapidly. This growth can be the result of either Zener breakdown or avalanche breakdown (the phenomenon of rapid splitting of electron-hole pairs).

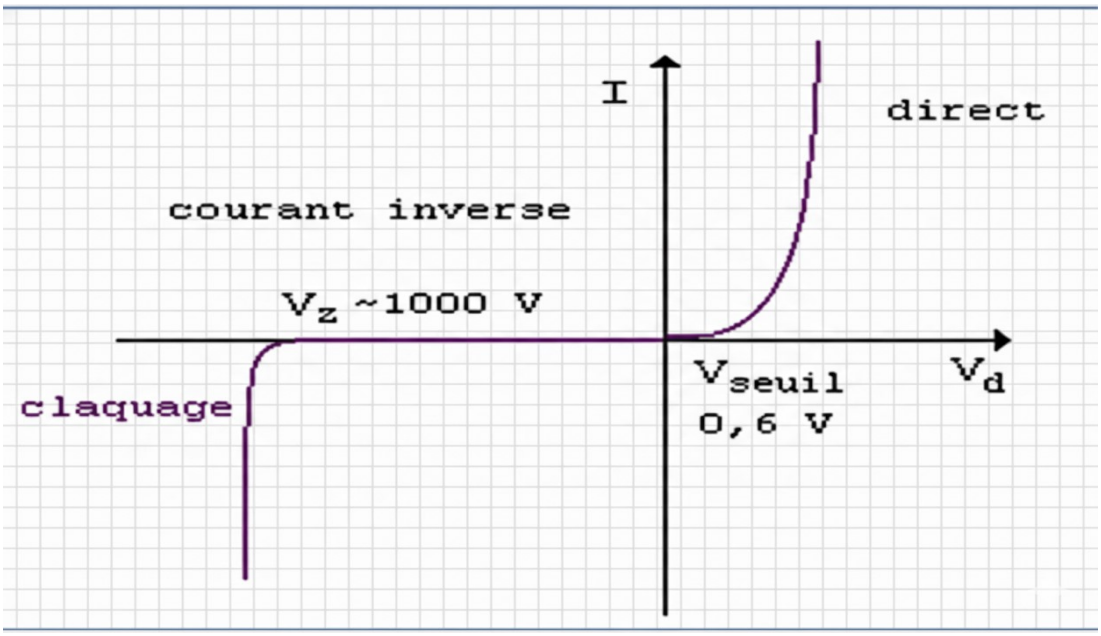


Figure 3.12: Representation of the diode operating zones (PN junction)

Chapter IV: The bipolar transistor "BJT"

Introduction

The bipolar transistor is an essential electronic component used in numerous applications, including amplification, switching, and signal processing circuits. This chapter provides a detailed overview of the structure, operation, configurations, characteristics with associated equations and applications.

4.1 Structures and Symbols of the Bipolar Transistor

A bipolar transistor consists of three layers of semiconductor material, typically silicon. N-type regions are doped with elements that provide additional electrons, while P-type regions are doped to create 'holes' (absence of electrons). A transistor is made up of three main regions: the emitter, base, and collector.

- **NPN Transistor:** A P-type layer (base) is placed between two N-type layers (emitter and collector).
- **PNP Transistor:** An N-type layer (base) is sandwiched between two P-type layers (emitter and collector).

Below are the basic illustrations of the two types of transistors NPN and PNP structure (left) and their symbols when used as circuit element (right). The arrow on the emitter lead indicates the direction of current flow when the emitter-base junction is forward-biased. For both types of transistors, the currents flowing through the emitter, base, and collector, denoted as I_E, I_B, and I_C, respectively, are considered positive when flowing into the transistor. The voltages V_{BE}, V_{CB}, and V_{CE} correspond to the base-emitter, collector-base, and collector-emitter voltages.

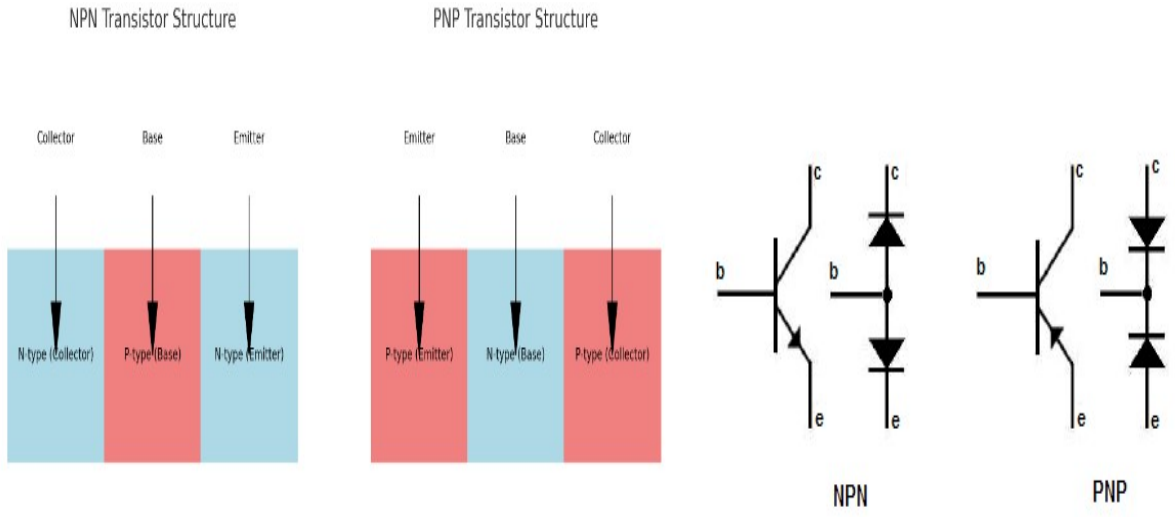


Figure 4.1: Illustrations of NPN and PNP transistor structures with their symbols

The evolution of semiconductor technology has been marked by groundbreaking advancements that have shaped modern electronics. From the invention of the point-contact transistor in the 1940s to the emergence of two-dimensional materials in recent years, each innovation has contributed to the miniaturization, efficiency, and functionality of electronic devices. The table below summarizes the key methods and technologies in semiconductor development, highlighting their characteristics, applications, and historical significance.

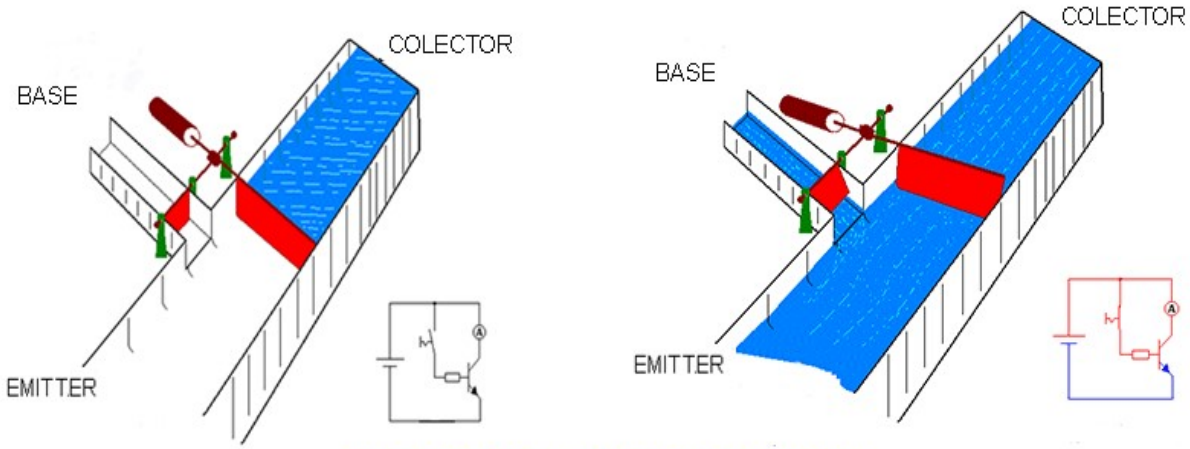
Era	Technology/Method	Key Characteristics	Applications	References
1940s-1950s	**Point-Contact Transistors**	Early form of transistors; fragile and low reliability.	 Radios, hearing aids.	Bardeen & Brattain (1947), Bell Labs.
1950s	**Junction Transistors**	More robust and efficient than point-contact transistors.	Early computers, amplifiers. 	Shockley (1951), Bell Labs.

1960s	**Planar Process (Bipolar Junction Transistors)**	Developed by Jean Hoerni; allowed for mass production and integration.	Integrated Circuits (ICs).	Hoerni (1959), Fairchild Semiconductor.
1970s	**MOSFET (Metal-Oxide-Semiconductor Field-Effect Transistor)**	Enabled high-density integration of transistors on chips.	Microprocessors, memory chips.	Kahng & Atalla (1960), RCA Labs.
1980s	**CMOS (Complementary Metal-Oxide-Semiconductor)**	Low power consumption; dominant technology for digital ICs.	Microcontrollers, mobile devices.	Mead & Conway (1980), VLSI Revolution.
1990s	**SOI (Silicon-on-Insulator)**	Reduced parasitic effects and power leakage.	High-speed processors.	Tsu-Jae King Liu (1998), UC Berkeley.
2000s	**High-k/Metal Gate Technologies**	Improved transistor scaling and reduced leakage currents.	Advanced microprocessors.	Intel & IBM Collaborations (2007).
2010s	**FinFET (Fin Field-Effect Transistor)**	3D structure for higher performance and power efficiency.	Modern CPUs and GPUs.	Hu et al. (2011), Intel.
2020s	**Gate-All-Around (GAA) Transistors**	Further miniaturization and power efficiency; successor to FinFET.	AI accelerators, quantum computing.	Samsung & TSMC (2022).
Present	**2D Materials and Nanotechnology**	Use of graphene, MoS_2, and other materials for ultra-small and energy-efficient transistors.	Emerging applications in IoT, AI, and beyond.	Geim & Novoselov (2010), Nobel Prize.

Table. 4.1 The key methods and technologies in semiconductor development

4.2. BJT polarization: how a small signal controls large current flow?

To make a bipolar junction transistor operate correctly, it must be polarized, meaning specific voltages are applied to its terminals to enable current flow. This setup is crucial for the BJT to work as either an amplifier or a switch, and the approach differs slightly for NPN and PNP transistors. The illustration of figure 4.2 shows how a bipolar junction transistor operates using an analogy of water flow to represent the behaviour of electric current in the transistor. This diagram uses a water analogy to explain how a BJT works, showing how a small control action can regulate a larger flow of current. In each illustartion, the blue area represents the flow of current through the transistor, while the red paddle or switch connected to the base serves as a control mechanism. Think of it as a small valve that either blocks or allows the flow of water (current) in the main pipe. The pipes represent different regions of the transistor: the emitter, base, and collector.



https://www.infootec.net/bipolar-transistor-bjt/

Figure 4.2: Understanding bipolar junction transistor operation through a water flow analogy.

According to the left diagram "Off State", the base switch is open. No current flows into the base, which means the flow of water (or current) from the collector to the emitter is blocked. This setup shows the transistor in an "off" state, where it acts as a barrier, preventing any current from flowing through the main circuit.

Essentially, without any input at the base, the transistor prevents the larger current from moving across the collector-emitter path. In the right diagram **"On** State", the base switch is closed, allowing a small amount of water (current) to flow into the base. This small base current enables a larger current to flow from the collector to the emitter, just as opening a small valve could allow a main water flow to continue downstream. In this "on" state, the transistor allows the main current to pass through the collector and emitter freely, controlled by the small current that's applied at the base.

Under each water analogy is a simplified electrical circuit. It shows the base (B), collector (C), and emitter (E) connections, with a power source attached to the collector and a ground connected to the emitter. In both diagrams, the switch in the base circuit illustrates that a small base voltage (when the switch is closed) controls the larger collector-emitter current.

4.2.1 Polarizing an NPN transistor

- **Base-emitter junction**: This junction needs to be forward-biased. To do this, a small positive voltage is applied to the base relative to the emitter. This setup allows electrons to move from the emitter (an N-type region) toward the base (a P-type region).
- **collector-base junction**: Here, the goal is to reverse-bias the junction, which means applying a larger positive voltage to the collector relative to the base. This reverse bias encourages electrons to travel from the base to the collector, facilitating a flow of current from collector to emitter.

In action: When an NPN transistor is polarized in this way, a small current entering the base makes it possible for a much larger current to flow from the collector to the emitter. This ability to control a larger current with a smaller one is the key to its amplifying or switching functions.

4.2.2 Polarizing a PNP transistor

- **Base-emitter junction**: Like with the NPN, the base-emitter junction must be forward-biased, but in a PNP transistor, the base is made slightly negative relative to the emitter. This allows positive charge carriers, called holes, to move from the emitter (P-type) to the base (N-type).
- **Collector-base junction**: This junction is reverse-biased by applying a more negative voltage to the collector compared to the base. This reverse bias facilitates the flow of current from the emitter to the collector.

In action: When a PNP transistor is polarized correctly, a small current flowing out of the base enables a larger current to pass from the emitter to the collector, allowing it to control a larger current with a smaller one just as with the NPN.

4.3 Study of the transistor's currents

The relationships between the currents in a Bipolar Junction Transistor are fundamental to understanding its operation. These are based on the three main currents in a transistor: the base current (I_B), the collector current (I_C), and the emitter current (I_E). In the following, we discuss the primary relationships:

a. Basic Relationship

At its core, a transistor follows the principle of current conservation: the total current entering equals the total current leaving. This means:

$$I_E = I_C + I_B \qquad \textbf{(4.1)}$$

This relationship holds true for all modes of operation.

b. Collector current and gain

When the transistor is in its active mode (used for amplification), the collector current depends on the base current and a factor called the current gain (β):

$$I_C = \beta I_B \quad \textbf{(4.2)}$$

Where, β is the transistor's current gain, usually a large number (e.g. **100-300**). So, a small base current is "multiplied" by β to produce a larger collector current. This is what makes BJTs effective as amplifiers.

c. Emitter current and total gain

The emitter current can also be expressed in terms of the base current and the transistor's total gain (**α**), where α is related to β as follow:

$$\alpha = \frac{\beta}{1+\beta} \quad \textbf{(4.4)}$$

Using this relationship, the emitter current can be written as:

$$I_E = (1 + \beta) I_B \quad \textbf{(4.5)}$$

This shows that the emitter current is slightly larger than the collector current due to the additional base current.

d. Saturation currents (leakages)

Leakage current, in the context of electrical systems and circuits, refers to the small amount of current that flows through a circuit even when it is not supposed to be active or when a device is turned off. This can happen for various reasons, depending on the system. In a transistor, even when it is in the "cutoff" state (off mode), there may still be a minimal current flowing between the collector and emitter due to leakage in the base-emitter junction or imperfections. This residual current is very small but can affect sensitive circuits, especially in low-power devices.

Even when a transistor is "off" or in cutoff mode, small leakage currents can flow:

- ✓ **I_{CB0}:** The saturation current of the collector-base junction when I_E=0 (in the case of a common-base configuration).
- ✓ **I_{EB0}:** The saturation current of the emitter-base junction when I_C=0 (in the case of a common-collector configuration).
- ✓ **I_{CE0}:** The saturation current of the collector-emitter junction when I_B=0 (in the case of a common-emitter configuration).

These currents are usually very small but can still be important in precision or low-power circuits.

- **Common-base configuration** : $I_C = \alpha I_E + I_{CB0}$
- **Common-emitter configuration** : $I_C = \beta I_B + = I_{CE0}$
- **Common-collector configuration** : $I_E = \gamma I_B + I_{EB0}$

At low temperature the leakage currents are zero.

$$\alpha = \frac{I_C}{I_E},\ \beta = \frac{I_C}{I_B} \text{ and } \gamma = \frac{I_E}{I_B} \qquad \textbf{(4.6)}$$

Where: $\alpha < 1$, $\beta \gg 1$ and $\gamma \gg 1$

$$\alpha = \frac{\beta}{1+\beta},\ \beta = \frac{\alpha}{1+\alpha},\ \gamma = 1 + \beta = \frac{1}{1-\alpha}$$

Subsequently, we can deduce:

$$I_{CE} = (1+\beta) I_{CB} \qquad \textbf{(4.7)}$$

Remark: When the temperature increases by **5°C**, the residual currents increase by **one unit**.

4.4 Ebers-Moll model

The Ebers-Moll model provides a comprehensive mathematical representation of a bipolar junction transistor by considering it as two coupled diodes with controlled current flow. The model accurately describes the behavior of the BJT in all its regions of operation (active, saturation, and cutoff). Bellow a detailed explanation and demonstration.

For an NPN transistor, the Ebers-Moll model defines the emitter and collector currents as:

$$I_E = [I_{ES}\exp\left(\frac{V_{BE}}{V_T}\right) - 1] - [\alpha_R I_{CS}\exp\left(\frac{V_{BC}}{V_T}\right) - 1] \quad \textbf{(4.8)}$$

$$I_C = [\alpha_F I_{ES}\exp\left(\frac{V_{BE}}{V_T}\right) - 1] - [I_{CS}\exp\left(\frac{V_{BC}}{V_T}\right) - 1] \quad \textbf{(4.9)}$$

$$I_B = I_E - I_C \quad \textbf{(4.10)}$$

Where:

- $\mathbf{I_{ES}}$, $\mathbf{I_{CS}}$: Reverse saturation currents of emitter-base and collector-base diodes
- $\mathbf{V_{BE}}$, $\mathbf{V_{BC}}$: Base-emitter and base-collector voltages
- $\mathbf{V_T}$: Thermal voltage (~25.85 mV at room temperature)
- $\boldsymbol{\alpha_F}$: Common-base forward current gain (typically ~0.99)
- $\boldsymbol{\alpha_R}$: Common-base reverse current gain (typically ~0.5–0.8)

The equivalent circuit includes two diodes (base-emitter and base-collector) and two current sources representing $\alpha_F I_E$ and $\alpha_R I_c$. This allows modeling of both injection and recombination effects.

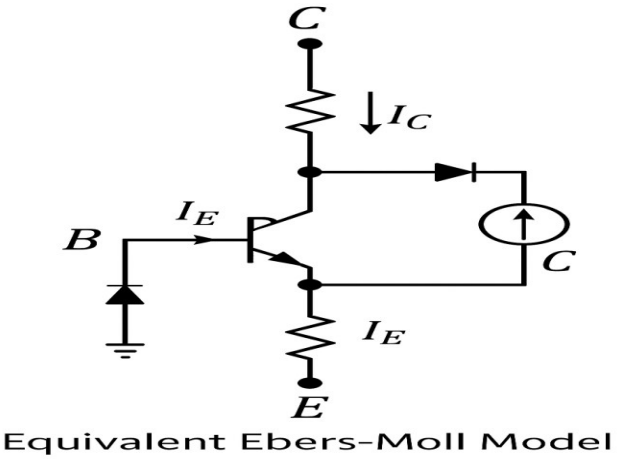


Figure 4.3: Equivalent Ebers-Moll model circuit diagram.

4.5 Modes of operation

Typical BJT operating regions are described by junction biases as follows:

- Active Mode: $V_{BE} > 0$, $V_{BC} < 0$
- Saturation Mode: $V_{BE} > 0$, $V_{BC} > 0$
- Cut-off Mode: $V_{BE} < 0$, $V_{BC} < 0$
- Reverse Active: $V_{BE} < 0$, $V_{BC} > 0$

The model supports all transistor operation modes including cutoff, forward active, saturation, and reverse active. These are defined based on the biasing of VBE and V_{BC}. In forward active mode, the model simplifies to:

$$I_c = \beta I_B = \alpha_R I_c \approx \beta I_B = \alpha_F I_E \quad \textbf{(4.11)}$$

The emitter current follows:

$$I_E = [I_{ES} \exp\left(\frac{V_{BE}}{V_T}\right) - 1] \text{ and } \beta = \frac{\alpha_F}{1-\alpha_F} \quad \textbf{(4.12)}$$

Applications of Ebers-Moll model include circuit simulations, nonlinear dc analysis, and spice modeling. Limitations include the lack of high-frequency effects and parasitic modeling, which are covered by advanced models like Gummel-Poon.

4.5.1 Current-voltage characteristics

The current-voltage (I-V) characteristics of a BJT represent the relationship between the current flowing through the transistor and the voltage applied across its terminals. When a small current is applied to the base, it controls the larger current flowing from the emitter to the collector. The current-voltage characteristics are crucial for understanding how it operates in a circuit. These characteristics also help to visualize and understand how a BJT behaves under different operating conditions. Furthermore, the I-V characteristic curve helps engineers design circuits by indicating the operating points of a BJT, showing regions of amplification, saturation, and cutoff, which are vital for applications like amplification, switching, and signal modulation. We can study these characteristics by considering the transistor as a two-port network model and hybrid parmeters (**h-parameters**).

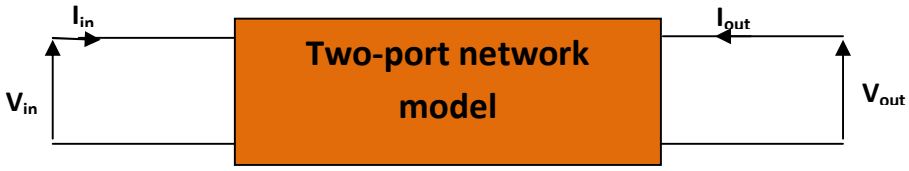


Figure 4.4: Two-port network model

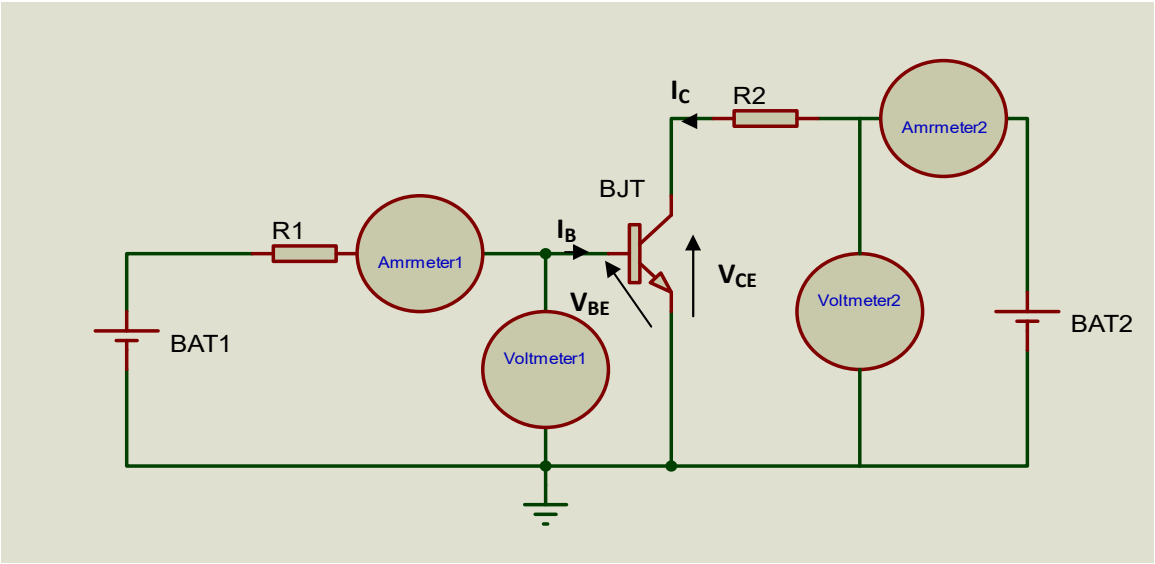


Figure 4.5: Polarization circuit of BJT transistor

The h-parameters are a set of four parameters (h_{11}, h_{12}, h_{21} , h_{22}) used to:

- Describe the behavior of a BJT in terms of small-signal analysis.
- Provide a convenient way to model a transistor's behavior in various configurations (e.g., common emitter, common base, or common collector).
- They simplify transistor circuit analysis by breaking it into manageable linear equations.
- Widely used in low-frequency small-signal analysis.
- They can be measured directly and are often provided in transistor datasheets.

These parameters are derived from the relationships between the input voltage, input current, output voltage, and output current of the transistor as follows:

$$\begin{pmatrix} V_{in} \\ I_{out} \end{pmatrix} = f \begin{pmatrix} I_{in} \\ V_{out} \end{pmatrix} \quad ; \quad \begin{pmatrix} V_{BE} \\ I_C \end{pmatrix} = \begin{bmatrix} h_{11} & h_{12} \\ h_{21} & h_{22} \end{bmatrix} \begin{pmatrix} I_B \\ V_{CE} \end{pmatrix} \tag{4.13}$$

Where :

- h_{11}**Input Impedance (h-input):** Defined as the small-signal input impedance with the output short-circuited. It gives the input resistance of the transistor in Ohms.

$$h_{11} = \left.\frac{V_{BE}}{I_B}\right|_{V_{CE}=0} \tag{4.14}$$

- h_{12} **Reverse Voltage Gain (h-reverse transfer):** Represents the feedback effect from the output to the input. Usually has a very small value because BJTs typically exhibit minimal reverse coupling.

$$h_{12} = \left.\frac{V_{BE}}{V_{CE}}\right|_{I_B=0} \tag{4.15}$$

- h_{21} **Forward Current Gain (h-forward transfer):** Describes the current gain of the transistor when the output is open-circuited. This is often the largest h-parameter, as BJTs are designed to amplify current.

$$h_{21} = \frac{I_C}{I_B}\Big|_{V_{CE}=0} \quad \textbf{(4.16)}$$

- h_{22} **Output Admittance (h-output):** Defined as the small-signal output admittance with the input open-circuited. It gives an idea of the output resistance, as admittance is the reciprocal of resistance.

$$h_{22} = \frac{I_C}{V_{CE}}\Big|_{I_B=0} \quad \textbf{(4.17)}$$

I-V characteristics of the BJT typically involve:

1. **V_{BE} vs. I_B**: In the active region, as the base-emitter voltage increases beyond a threshold (around 0.7V for silicon BJTs), the base current increases exponentially, which in turn controls the larger collector current.
2. **V_{CE} vs. I_C**: The collector current is primarily determined by the base current in the active region. However, in the saturation region, as the collector-emitter voltage decreases, the transistor becomes fully "on," and the collector current levels off, indicating maximum current flow.
3. **Cut-off region**: When the base-emitter voltage is below the threshold (typically below 0.7V for silicon), the transistor enters the cutoff region, where both the base and collector currents are near zero, and the transistor is effectively "off."
4. **Saturation region**: When both the base-emitter voltage and collector-emitter voltage are high enough, the transistor enters saturation, where it behaves like a closed switch with maximum current flowing from collector to emitter, regardless of small changes in V_{CE}.

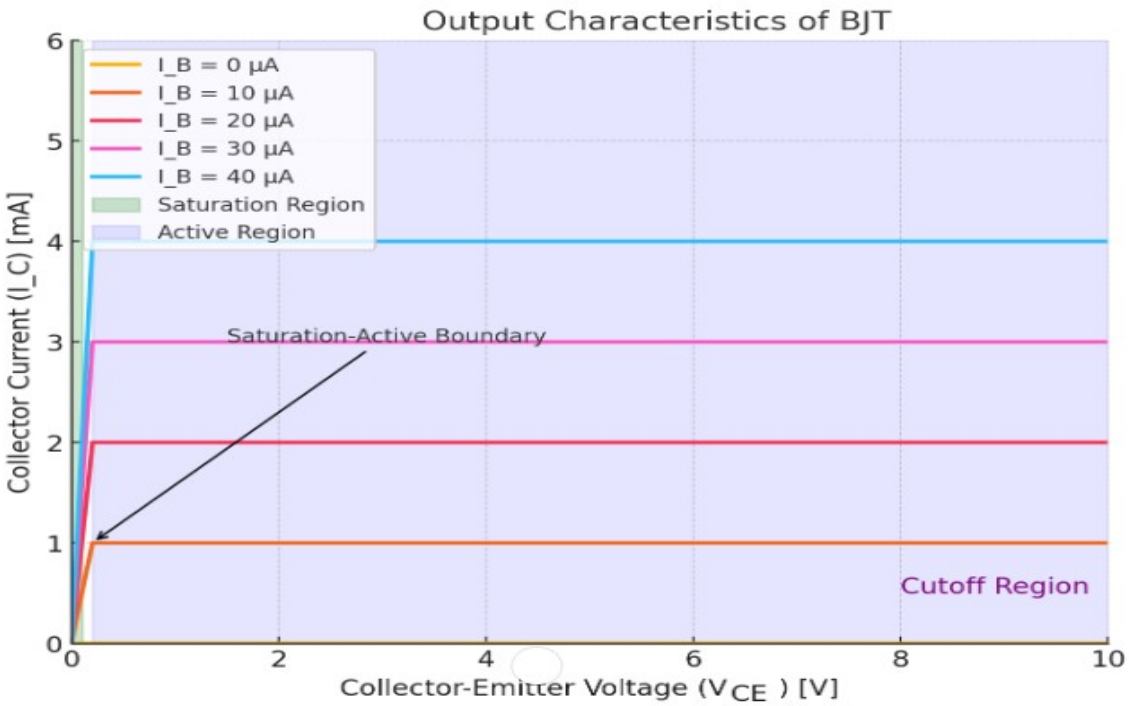


Figure 4.6: I-V characteristics of BJT transistor

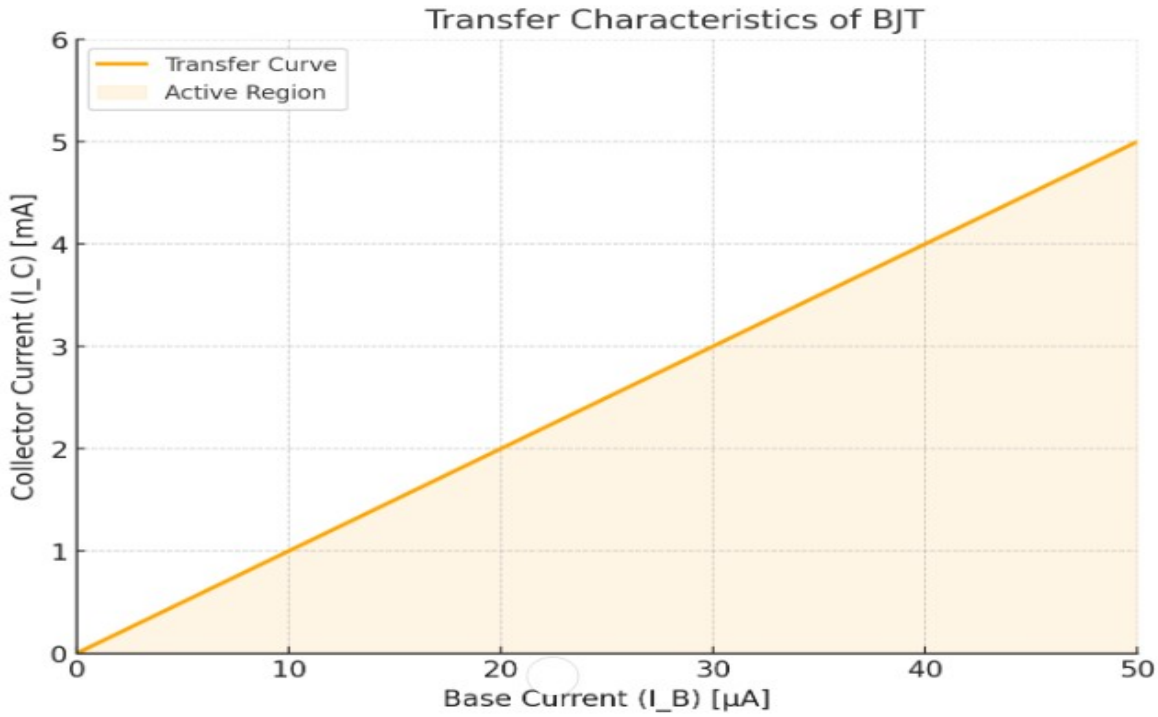


Figure 4.7: I-V transfer characteristics of BJT transistor

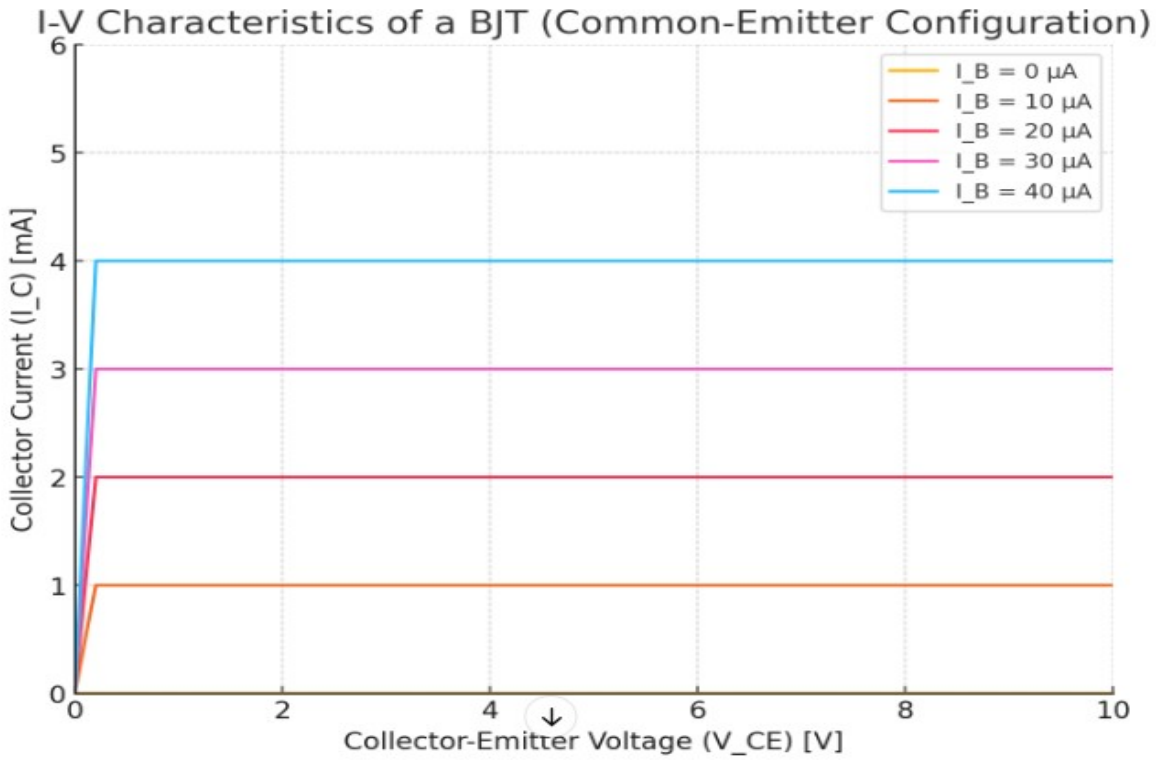


Figure 4.8: I-V characteristics of BJT transistor as common emitter configuration.

4.5.2 Operating modes of the BJT

To understand how a BJT transistor works, we need to look at the different ways it can operate, or "regimes." Each regime depends on how the voltages are applied across the BJT's terminals and dictates whether the transistor is "off," amplifying, or "fully on". These regimes are called: **cut-off**, **active** and **saturation**. Let's go through each one with simple explanations and equations.

a. Cutoff region - transistor off

In the cutoff region, the BJT is effectively off, like an open switch. Here, there's no current flowing through the transistor from the collector to the emitter because there's no current flowing into the base. The base-emitter junction isn't forward-biased, so it doesn't let any current through. Without base current, the transistor can't turn on the larger collector-emitter current.

- **Conditions**

- The base-emitter voltage $\mathbf{V_{BE}}$ is less than 0.7V (for a silicon transistor).
- Base current $\mathbf{I_B}$ is zero so $\mathbf{I_C}$ is also equal to zero.

So, when $\mathbf{V_{BE}}$ is too low, there's no current flow, and the transistor stays off.

b. Active region - transistor amplifying

In the active region, the BJT is "On" in a way that allows it to amplify signals. A small current entering the base creates a larger current between the collector and emitter. This is the mode used for amplification. The base-emitter junction is forward-biased (about 0.7V for silicon), allowing current to flow into the base. This small base current controls a much larger collector current, making it possible to amplify signals.

- **Conditions**

a. Base-emitter voltage $\mathbf{V_{BE}}$ is about 0.7V

b. Collector-emitter voltage $\mathbf{V_{CE}}$ is higher than $\mathbf{V_{BE}}$

When these two conditions are verified, the output currents are: $I_c = \beta I_B$ and $I_E = I_B + I_C = (I_B + \beta I_B) \approx (1 + \beta) I_B$

c. Saturation region - transistor fully on

In saturation region, the BJT behaves like a fully closed switch. Current flows freely from the collector to the emitter, with very little resistance. This is useful when you want the transistor to function as a switch, simply turning the current on or off. Both the base-emitter and base-collector junctions are forward-biased. So, the transistor lets as much current as possible flow from the collector to the emitter.

- **Conditions**:
  - V_{BE} is around 0.7V, and V_{CE} is very low (around 0.2V or less).
  - The base current I_B is large enough to push the collector current I_C to its maximum.

For the output current we have: $I_c \approx I_{sat}$ and $I_c < \beta I_B$

Remark: In saturation mode, the relationship $I_c = \beta I_B$ no longer holds exactly; instead, the collector current hits a maximum value (determined by the circuit) and stays there. Increasing the base current won't increase the collector current any further.

Region	*Transistor behavior*	*Base-Emitter Voltage (V_{BE})*	*Collector-Emitter Voltage (V_{CE})*	*Main Equations*
Cutoff	Transistor is "off"	Less than 0.7V	Any	$I_B = 0$, $I_C = 0$
Active	Transistor is "amplifying"	Around 0.7V	Greater than V_{BE}	$I_C=\beta I_B$
Saturation	Transistor is "fully on" (like a switch)	Around 0.7V	Less than 0.2V	$IC \approx I_{Csat}$

Table. 4.2 Summary of operating modes of bipolar junction

4.6 Applications of bipolar transistors

The bipolar junction transistor (BJT) is a foundational workhorse of modern electronics, finding critical applications wherever signal control or amplification is required. Its fundamental ability to use a small current at its base to regulate a much larger current between its collector and emitter makes it incredibly versatile. This principle is exploited in amplifiers for audio systems, radios, and telecommunication devices, where it meticulously boosts weak signals without significantly distorting them.

Furthermore, operating at the extremes of its characteristics, the BJT serves as a highly efficient, fast-acting switch in digital logic circuits, power regulators, and pulse generators. While other technologies like MOSFETs now dominate high-density integrated circuits, the bipolar transistor remains indispensable in high-frequency analog applications, power electronics, and as a robust, reliable component in countless consumer and industrial systems.

- **Amplifiers:** In audio amplifiers, NPN transistors are often used to amplify audio signals, allowing for the driving of speakers,
- **Logic circuits:** Transistors are essential in the design of digital circuits, particularly in logic gates like: AND, OR, and NOT.
- **Switching power supplies:** Used to regulate and convert energy in switching power supplies, they offer increased efficiency,
- **Detectors and Sensors:** Transistors amplify weak signals in devices such as light or temperature sensors.

Chapter V: Junction Field Effect Transistor « JFET»

Introduction

Field effect transistors: FET are semiconductor devices controlled transversely by voltage. Only the majority carriers (electrons or holes) are involved in their operation, hence the name unipolar transistor. Unlike the bipolar transistor which is a current-controlled device. It has three electrodes (ohmic contacts) where two are arranged at the ends: Drain (D), Source (S) and the third called Gate (G) placed laterally. By applying a transverse electric field (voltage V_{GS}) at the gate, the flow of charge carriers through the transistor channel can be controlled.

TECs are classified into three main families:

- Semiconductor junction FET commonly called JFET: Junction Field Effect Transistor.
- **FinFET**
- MESFET metal-semiconductor junction TEC.
- Insulated grid TEC such as:
  - **MOSFET**: Metal Oxide Semiconductor FET.
  - **HER**: Silicon On Nothing
  - **SELF**: Silicon On Insulator

Noticed

JFET and MESFET transistors have a completely comparable structure.

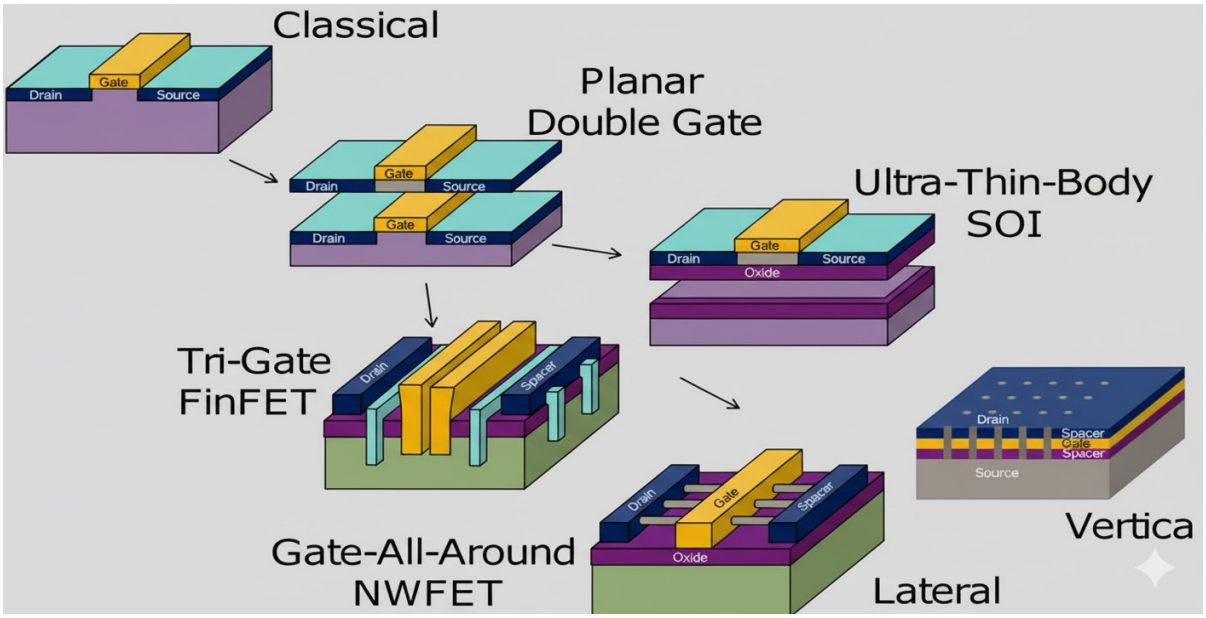


Figure 5.1: Evolution of FET technology

In this chapter we will focus on the study of the JFET transistor. All field-effect transistors, including JFETs, are classified as **unipolar devices** because their operation depends exclusively on the movement of a single type of charge carrier. In an N-channel JFET, only electrons participate in current conduction through the channel. In a P-channel JFET, only holes carry the current. This contrasts sharply with bipolar transistors, where both electrons and holes play essential roles in device operation.

The unipolar nature of JFETs provides several advantages. The absence of minority carrier injection and storage means that JFETs can switch faster than comparable bipolar devices. Additionally, the simpler carrier transport mechanism results in more predictable temperature characteristics and reduced sensitivity to radiation, making JFETs particularly suitable for space and military applications where radiation hardness is essential.

5.1. Comparative analysis: JFET vs. BJT vs. MOSFET

Understanding the JFET requires placing it in context with other transistor technologies. The following comparison highlights the distinctive characteristics of each device type:

Characteristic	BJT	JFET	MOSFET
Control Mechanism	Current-controlled	Voltage-controlled	Voltage-controlled
Carrier Type	Bipolar (electrons & holes)	Unipolar (electrons or holes)	Unipolar (electrons or holes)
Input Impedance	Low to Medium (kΩ)	Very High (GΩ)	Extremely High (TΩ)
Transconductance	High	Medium	Medium to High
Noise Level	Medium	Low	Medium
Operating Mode	Active (normally off)	Depletion (normally on)	Enhancement or Depletion
Gate Current	Significant (μA to mA)	Negligible (pA)	Negligible (fA)
Power Handling	High	Medium	Low to High
Switching Speed	Good	Excellent	Excellent
Temperature Stability	Moderate	Good	Good
Radiation Hardness	Low	High	Low
Cost	Low	Medium	Low
Integration Density	Medium	Low	Very High

Table 5.1: Comparative characteristics of BJT, JFET, and MOSFET devices.

The JFET occupies a unique position in this spectrum. While MOSFETs have dominated integrated circuit applications due to their scalability and ease of fabrication, JFETs remain the preferred choice for discrete analog applications requiring low noise, high input impedance, and excellent linearity.

5.2. Types and Symbols

Depending on the type of majority carriers ensuring the current in the transistor channel, there are two types of JFET transistor: the N-channel JFET and the P-channel JFET (see the following table).

N-channel JFET **P-channel JFET**

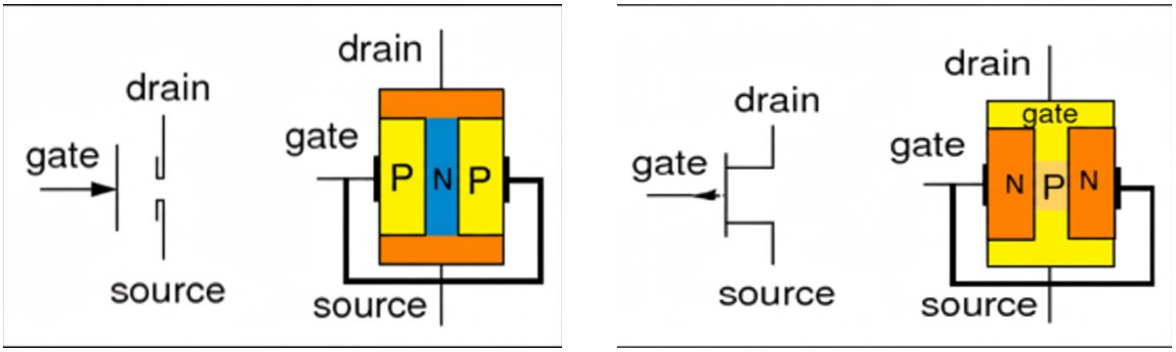


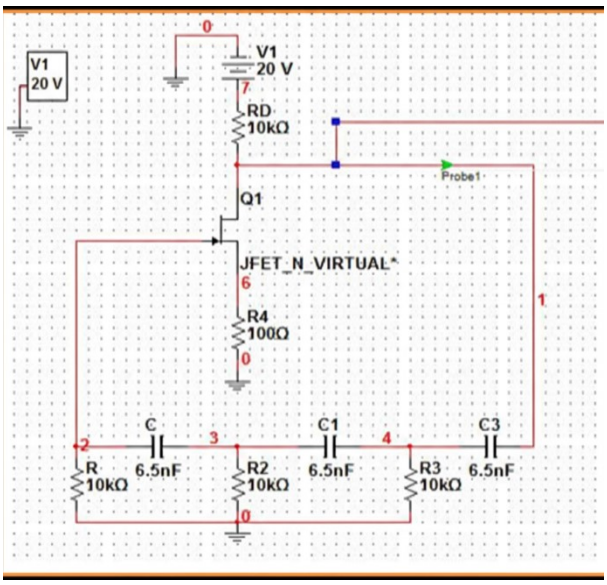
Figure 5.2: JFET types and symbols: n-JFET (left) and p-JFET (right)

Noticed: The arrow on the grid points in the direction of travel of the junction

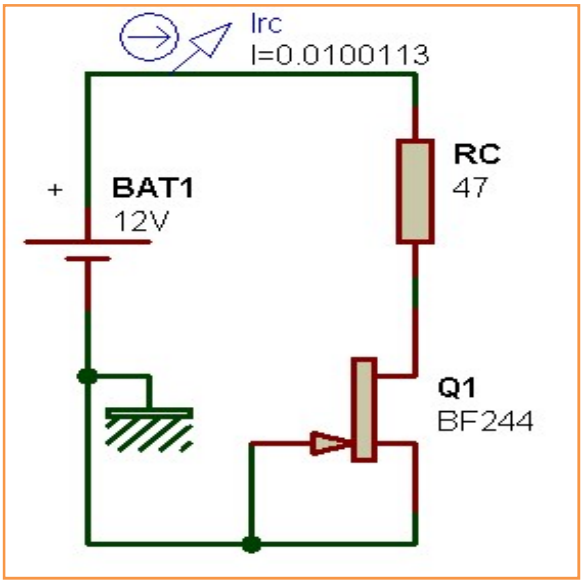
5.3. Characteristics and Applications of JFET

Compared to the bipolar transistor which contains two major sources of noise: thermal noise (generated by the base like all resistors) and shot noise (through the two junctions BC and BE), the JFET contains only one source of noise which is thermal noise (generated through the channel). Also, its physical dimensions are smaller than those of bipolar. In a portion of its current-voltage characteristic, called the Ohmic regime, the JFET behaves like a voltage variable resistor (VVR). It will take up less space in integrated circuits than a regular (discrete) resistor.

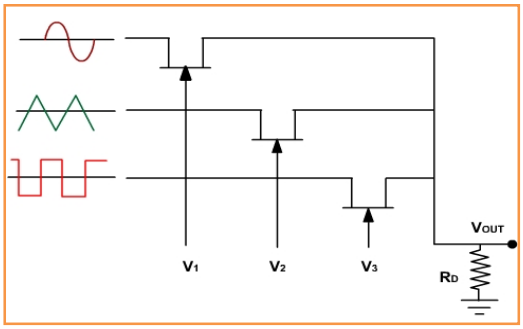
- Good current switching as well as its high dissipated power (amplifier).
- Has high input impedance.
- Can be used as a storage element in digital circuits (making RAM)
- Use as constant current source, cascode amplifier, chopper amplifier, phase shifting network oscillator, etc.
- In the operation of the mixer of FM and TV receivers.



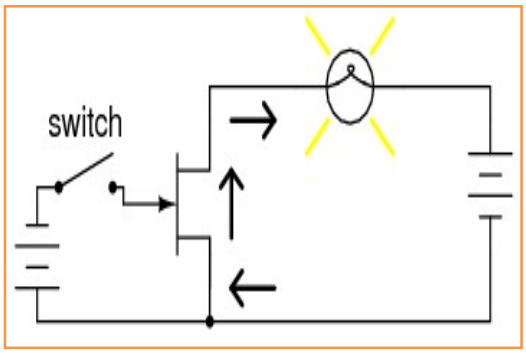
Phase-shifting network oscillator



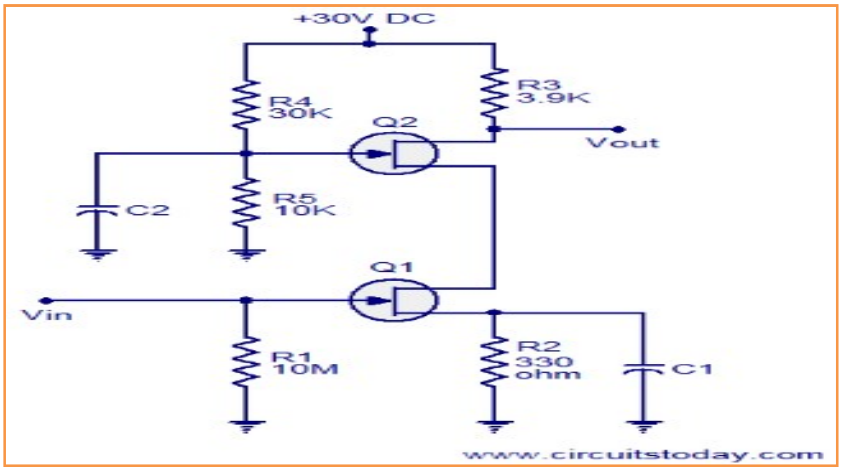
Current limiter



Multiplexer



JFET as a Switch



Cascade amplifier

Figure 5.3: Some JFET-based circuits

5.4. Physical description of the N-channel JFET structure

The physical structure of the N-channel JFET is shown in the figure below. A thin n-semiconductor layer is deposited on a P-type (lightly doped) semiconductor substrate. The drain and source are sometimes formed by two heavily doped (N^+) zones to make the Ohmic contacts. The gate is formed by a P-type semiconductor ring, made by diffusion, around the center of the channel, thus forming two PN junctions. The n-channel is therefore "sandwiched" by the gate. Also, the two space charge zones of the two diodes, with common cathode and anode, can modulate the channel thickness under the action of the voltage $V_{GS}<0$.

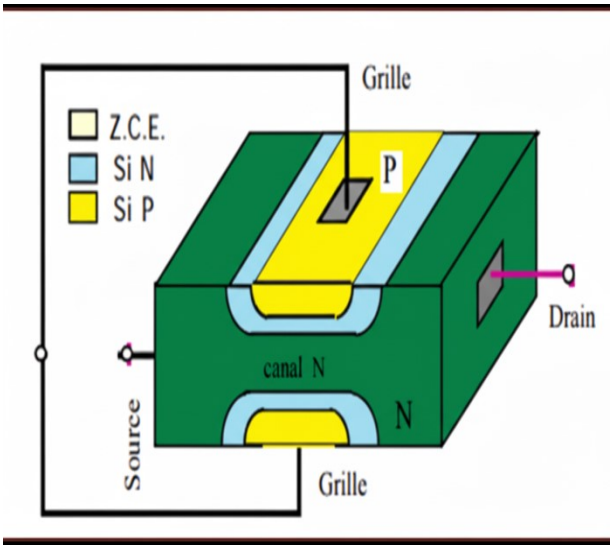


Figure 5.4: Physical structure of the JFET

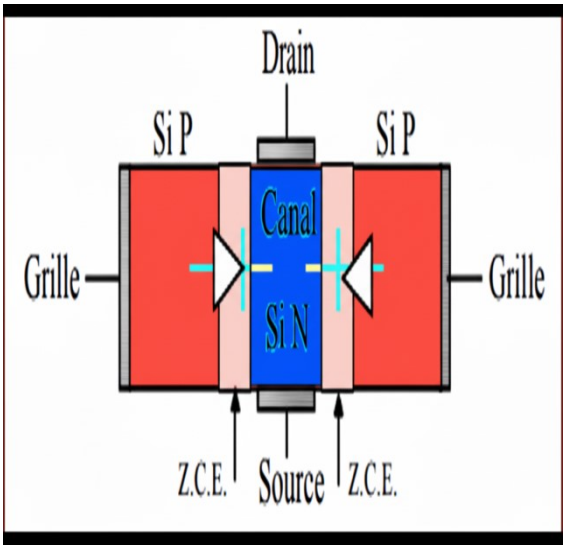


Figure 5.5: Channel level cutoff

5.5. Study of the static characteristics of the JFET

The static characteristics of a Junction Field-Effect Transistor (JFET) describe its DC behavior under steady-state conditions. These characteristics are fundamental to understanding how the JFET operates as a voltage-controlled device and are crucial for circuit design and biasing.

Primarily, two key sets of characteristics are studied:

5.5.1. Output or Drain Characteristics (I_n vs. V_{DS})

This graph plots the drain current (I_D) against the drain-to-source voltage (V_{DS}) for different constant values of gate-to-source voltage (V_{GS}).

- **Ohmic (Triode) Region**: At low V_{DS} (below pinch-off), I_D increases almost linearly with V_{DS} for a fixed V_{GS}. The channel acts like a voltage-controlled resistor. The slope here represents the channel resistance, controlled by V_{GS}.
- **Saturation (Active or Pinch-off) Region**: As V_{DS} increases further, it reaches a point ($V_{DSsat} = |V_P| - |V_{GS}|$) where the channel pinches off near the drain end. Beyond this point, I_D becomes relatively constant and almost independent of further increases in V_{DS}, but remains highly dependent on V_{GS}. This is the primary region used for amplification.
- **Breakdown Region**: If V_{DS} is increased excessively, the drain-to-gate junction breaks own, causing a rapid and destructive increase in I_D. This region must be avoided in normal operation.

The regions show that for a given V_{DS}, a more negative V_{GS} (for an n-channel JFET) reduces the drain current I_D. The curve for $V_{GS} = 0$ gives the maximum I_D (I_{DSS}).

5.4.2 Transfer Characteristic (I_D vs. V_{GS})

This graph plots the drain current against the gate-to-source voltage for a constant drain-to-source voltage chosen to be within the saturation region (e.g., $V_{DS} > |V_P|$).

The curve starts at I_{DSS} (the drain current when $V_{GS} = 0$) and decreases as V_{GS} becomes more negative (for n-channel). It ideally reaches zero at the pinch-off voltage (V_P or V_{GS} (off)), where the channel is completely depleted and conduction ceases. The relationship in the saturation region is approximately described by the square-law equation:

$$I_D = I_{DSS} \times (1 - V_{GS} / V_P)^2 \quad \textbf{(5.1)}$$

5.5.2. Significance of Studying Static Characteristics

- **Biasing**: Determines the stable operating point (Q-point) for amplification by setting appropriate V_{GS} and V_{DS} values.
- **Parameter Extraction**: Allows extraction of key device parameters like I_{DSS}, V_P (or V_{GS} (off)), and the transconductance ($g_m = \Delta I_D / \Delta V_{GS}$), which defines the gain.

  • Understanding Control: Clearly demonstrates the voltage-controlled nature of the JFET (V_{GS} controls I_D).
- **Region Identification**: Identifies the boundaries between the Ohmic, Saturation, and Breakdown regions, essential for selecting the correct operating mode.
- **Circuit Design**: Provides the foundational data needed to design amplifiers, switches, and other circuits using JFETs.

5.6. Polarization Modes

JFET biasing requires two power sources V_{DS} and V_{GS}. The sign of these sources depends on the JFET type. The following figure shows the bias modes for both n-channel and p-channel types.

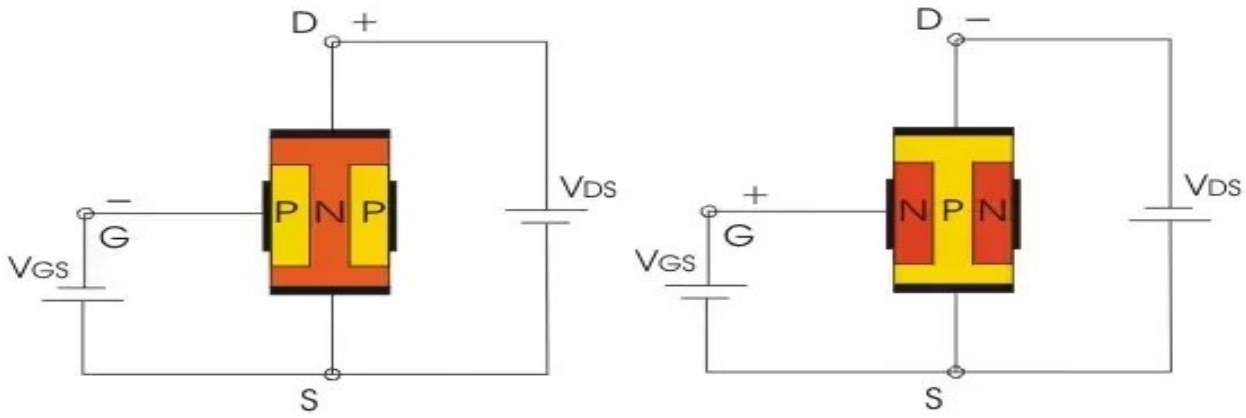


Figure 5.6: Polarization modes of the two types of JFET.

5.6.1. Static characteristics

The study of the static characteristics of the JFET transistor amounts to evaluating the evolution of the drain current as a function of the VDS voltage and the VGS voltage. These characteristics are two in number (see following figure):

- The direct characteristic: $I_D = f(V_{DS})|_{V_{GS}=cs}$
- The transfer characteristic: $I_D = f(V_{GS})|_{V_{DS}=cst}$

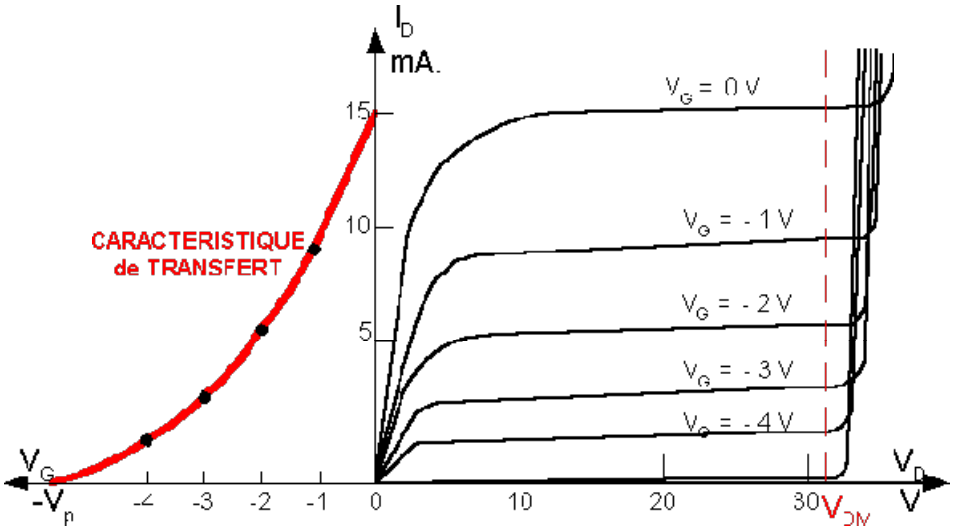


Figure5.7: Static characteristics of the JFET transistor

In this part we consider the study of the characteristics of the n-channel JFET (figure). We assume that:

- Both gate-channel junctions are assumed to be flat and abrupt.
- The doping of the N_D concentration channel is uniform.
- The mobility of electrons μ_n in the channel is considered constant and independent of the applied electric field (voltage).
- The length L of the channel is at least twice as long as its thickness 2e.

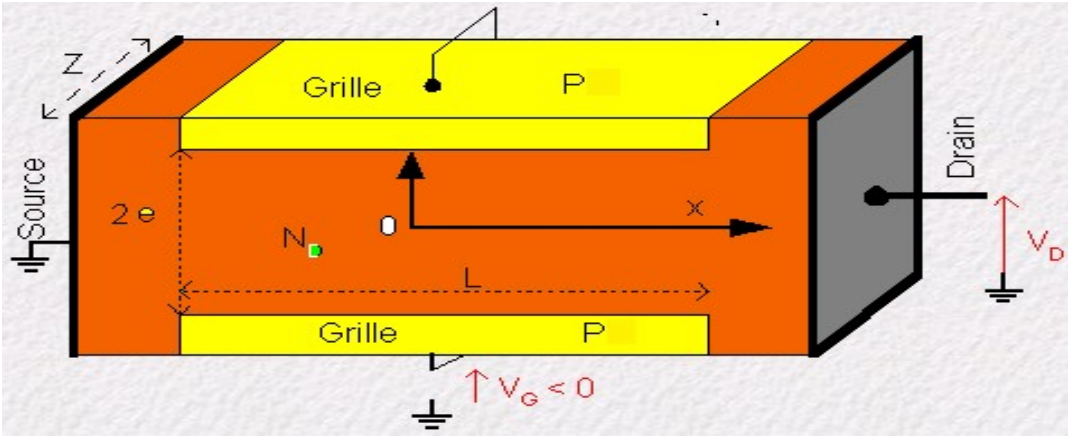


Figure 5.8: Symmetrical n-channel JFET.

Due to the VDS voltage, a potential $V(x)$ is produced in the channel, dependent on the abscissa, such that: $x \in [0 - L]$

$$V(x) = \begin{cases} 0 : potenteil\ à\ la\ source & pour\ x = 0 \\ V_D : potenteil\ à\ la\ source & pour\ x = L \end{cases} \quad (5.2)$$

Therefore the width of the ZCE "W ZCE" of each junction is not constant.

- In the absence of VGS voltage, is:W_{ZCE}

$$W_{ZCE} = \sqrt{\frac{2\varepsilon}{qN_D}(V_b + V(x))} \quad (5.3)$$

With represents the barrier voltage for the two junctions assumed to be identical.V_b

- In the presence of VGS<0,$W_{ZCE}$is worth:

$$W_{ZCE} = \sqrt{\frac{2\varepsilon}{qN_D}(V_b + V(x) - V_{GS})} \quad (5.4)$$

The resistance element dR, presented by a channel slice, located at the abscissa x and of thickness dx is:

$$dR = \frac{dx}{2\sigma_N Z.(e - W_{ZCE}(x))} \quad (5.5)$$

With σ_N represents the conductivity of electrons in the channel, such that:

$$\sigma_N = qN_D\mu_n \quad (5.6)$$

When this resistance element dR is crossed by the current ID, it results in a potential element dV expressed by:

$$dV = dR.I_D = \frac{dx.I_D}{2qN_D\mu_n.Z.(e - W_{ZCE}(x))} \quad (5.7)$$

Integrating this potential element over L amounts to writing: $dV(e - W_{ZCE}(x))$

$$\int_0^{V_D}(e - \sqrt{\frac{2\varepsilon}{qN_D}(V_b + V(x) - V_{GS})})dV = \int_0^L \frac{I_D}{2qN_D\mu_n.Z}dx \quad (5.8)$$

We set: $V_{P0} = \frac{qN_D.e^2}{2\varepsilon}$ and $g_0 = \frac{2qN_D\mu_n.Z.e}{L}$

With g_0 represents the channel conductance without considering the deserted area and the internal pinchoff voltage V_{P0}

Subsequently we can write:

$$I_D = g_0[V_D - \frac{2}{3V_{P0}^{\frac{1}{2}}}((V_D + V_b - V_{GS})^{\frac{3}{2}} - (V_b - V_{GS})^{\frac{3}{2}})] \quad \textbf{(5.9)}$$

Note: the remainder expression I_D is valid as long as $V_D < V_{Dsat}$, with V_{Dsa} represents the saturation voltage.

Direct characteristic:$I_D = f(V_{DS})|_{V_{GS}=cst}$

Analyzing the direct characteristic we can see four operating zones as shown in the figure 5.9.

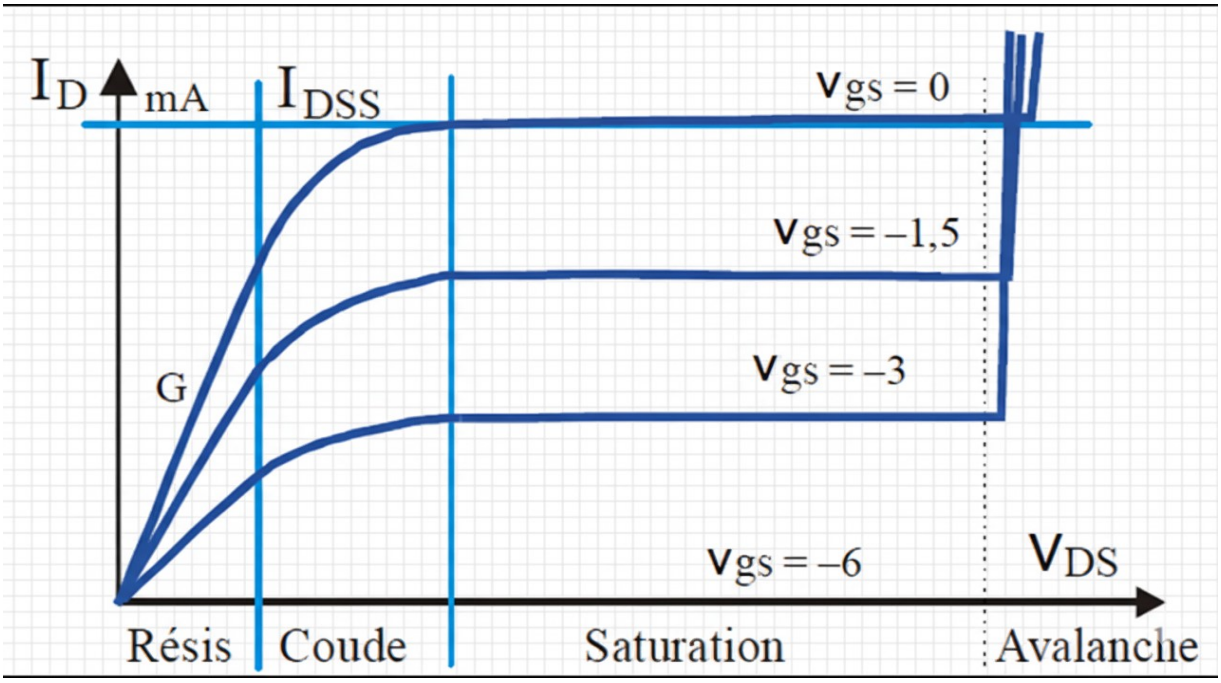


Figure 5.9: Representation of the four operating zones of the JFET

- **Ohmic Zone:** V_{GS}=0 and V_{DS}>0 (low)

In this area, for low values of the V_{DS} voltage, the I_D current varies linearly. In this case, the variation of the R_{DS} resistance is exploited and the channel behaves like

a variable resistor. The thickness "e" of the channel, which depends on the V_{GS} voltage, remains uniform and is even smaller when V_{GS} is negative.

For a certain voltage, called pinching, the channel pinches (I_D=0) and the transistor behaves like an open switch. The voltage equivalent to pinching is $V_P=V_{GSoff}$ (value given by the manufacturer).

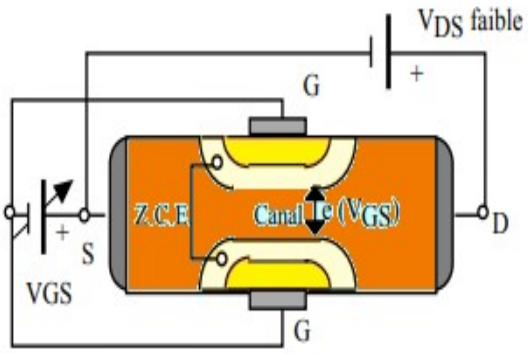


Figure 5.10: Representation of the JFET structure in the ohmic regime (for low V_{DS})

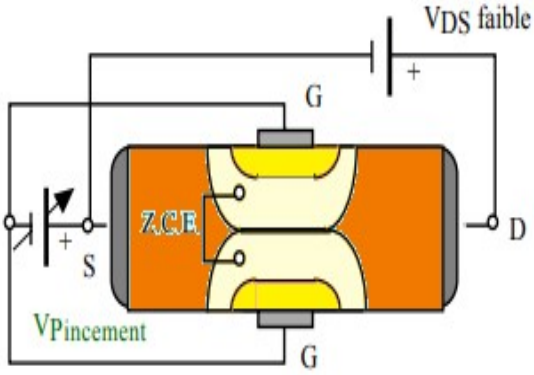


Figure 5.11: Representation of channel pinching (for low V_{DS})

In this case the R_{DS} resistance is expressed by the formula:

$$R_{DS} = \frac{R_{DS}}{1-K|V_{GS}|} \qquad (5.10)$$

With R_{DS} the value of R_{DS} for $V_{GS} = 0$ and K, expressed in V^{-1}, is a characteristic factor of the JFET.

- **Elbow area**: When V_{GS}<0 and V_{DS} increases

The thickness of the channel "e" will then depend on:

- The linear distribution of V_{DS} across the channel
- The V_{GS} voltage which will be used to create a space charge zone SCZ.

For example, let's apply a voltage V_{DS}=2V, the gate not being connected. The voltage is distributed linearly across the channel (see figure below).

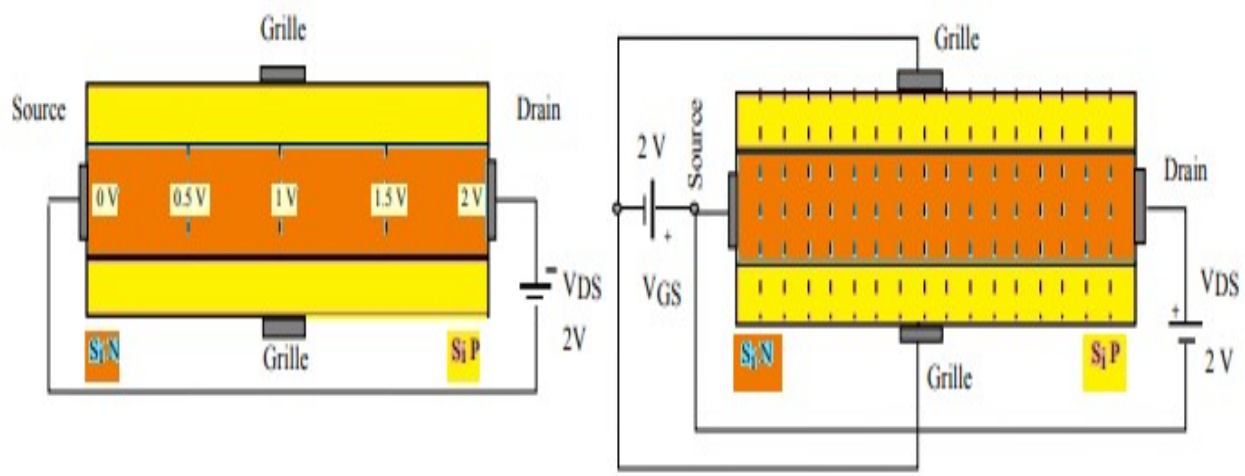


Figure 5.12: Representation of the JFET structure in the elbow region

Now let's apply a voltage V_{GS}=-2V>V_p and cut the channel to a set of n diodes (see figure). Taking into account the applied voltages, we give an electrical image of the reverse voltage of the diodes considered (**n=5**).

In this case, the diodes located near the drain are strongly blocked compared to diodes located near the source. The latter are subjected to a higher reverse voltage. The channel therefore tends to narrow on the drain side. The channel then takes the shape of a funnel. Its resistance is therefore no longer linear. This zone then corresponds to the beginning of the saturation regime.

The current in this area is expressed by the following equation:

$$I_D = \frac{I_{DSS}}{V_p^2}(1 - (V_{GS} - V_p)V_{DS} - V_{DS}^2) \quad \textbf{(5.11)}$$

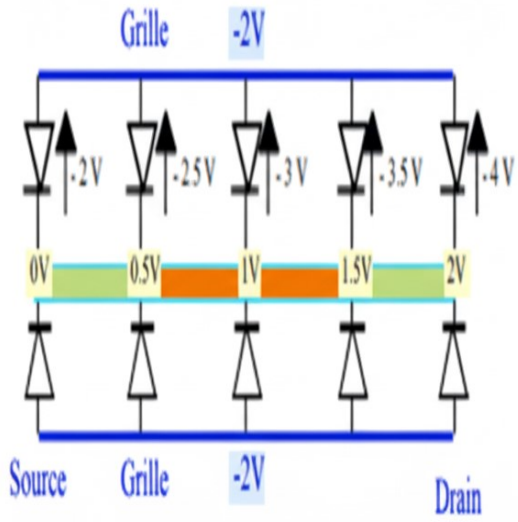


Figure 5.13 : Channel division into n- equivalent diodes

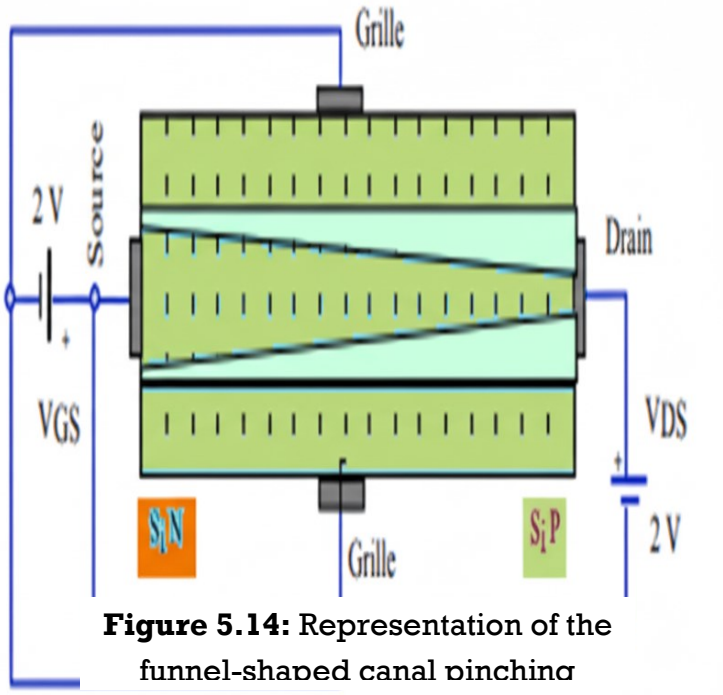


Figure 5.14: Representation of the funnel-shaped canal pinching

- **Saturation zone:** $V_{DS} \geq V_{DSsat} = V_{GS} - V_p$

When the voltage V_{DS} reaches its saturation value: $V_{DSsat} = V_{GS} - V_p$, the channel pinches again at point P_1. Unlike the pinch in the case of Ohmic regime, this local pinch does not cause the cancellation of the I_D current. At point P_1 the electrons acquire kinetic energy allowing them to reach the drain. In this case the current I_D reaches its maximum value I_{DSS} and the transistor is said to be saturated. The maximum value of I_D (for V_{GS}=0V) is I_{DSS} also provided by the manufacturer (**see the datasheet given in the figure 5.17).**

When $V_{DS} \geq V_{DSsat}$ the current I_D remains substantially constant, therefore the V_{DS}/R_{DS} ratio remains constant. Afterwards the pinch point P_1 moves to point P_2.

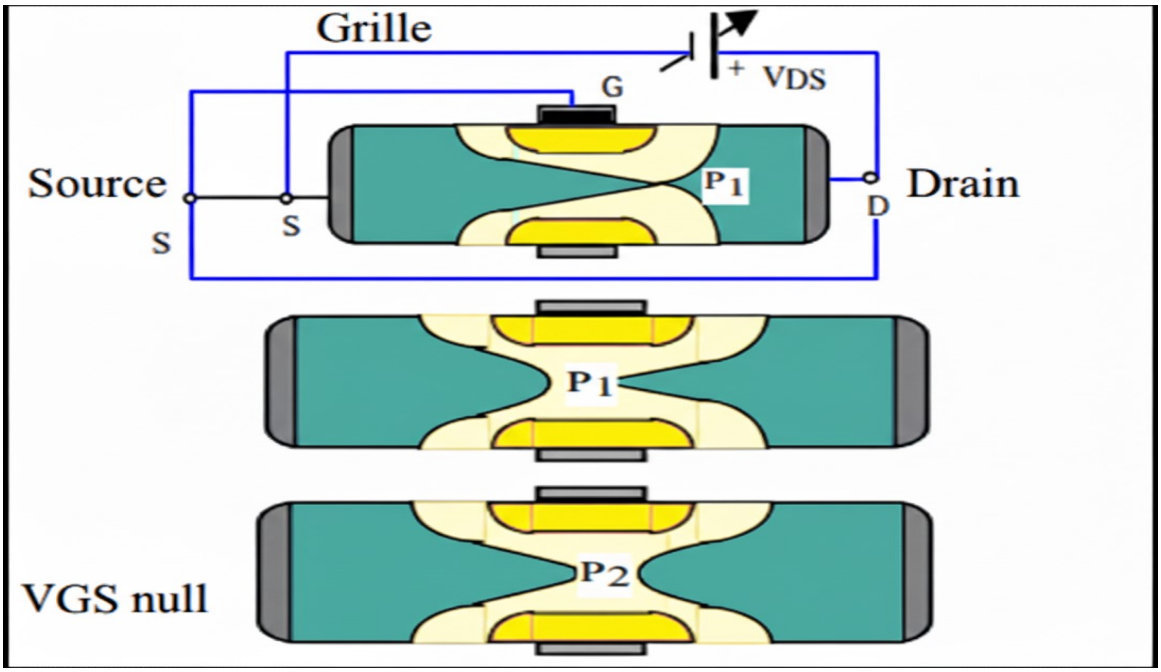


Figure 5.15: Representation of the JFET structure in the equivalent saturation regime

In this area, the expression of the evolution of the I_D current as a function of V_{DS} and V_{GS} is as follows:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 (1 - \lambda V_{DS}) \quad \textbf{(5.12)}$$

I_{DSS}: The maximum drain current (at V_{GS}=0)

With λ (expressed in V^{-1}) is a parameter linked to the current source and modelling the Early effect.

- **Avalanche zone: High VDS**

It results from a reverse breakdown of the drain-gate junction due to a rapid increase in the I_D current (splitting of the charge carriers). If the I_D current is not limited, this breakdown becomes destructive to the transistor.

Transfer characteristic: $I_D = f(V_{GS})|_{V_{DS}=cst}$

The transfer curve given in the figure below is very useful for the operation of the JFET in linear amplification.

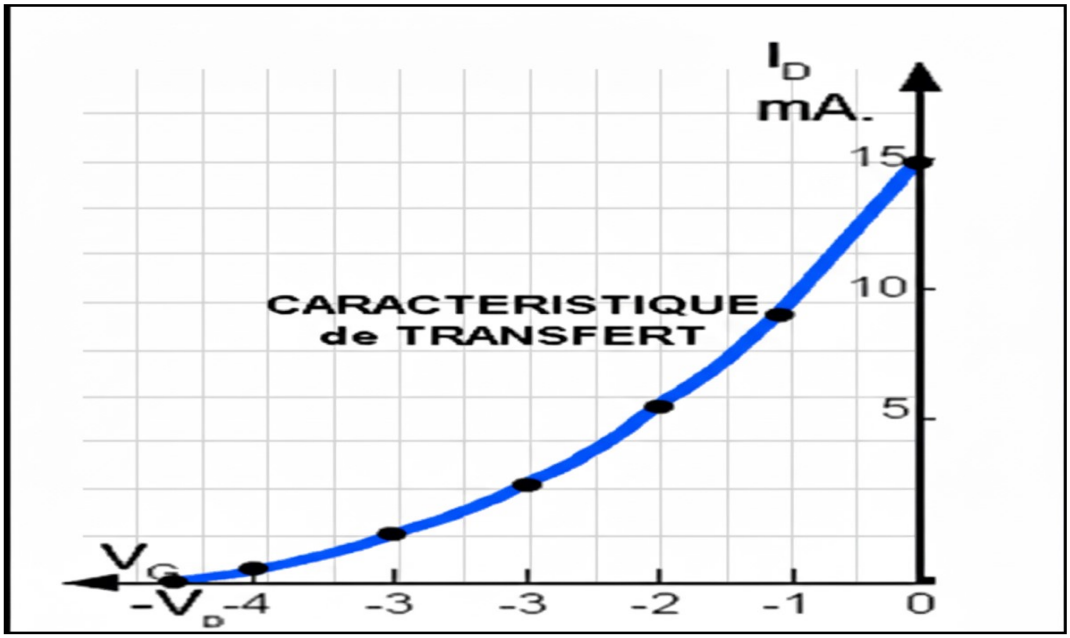


Figure 5.16: Transfer characteristic of JFET

From the transfer characteristic, we define the transconductance as: g_m

$$g_m = \frac{\partial I_D}{\partial V_{GS}} \tag{5.13}$$

Canal pinching occurs when: $V_{Dsat} = V_{p0} - V_b - V_{GS}$

For this condition, the expression of the saturation current I_{Dsat} (as a function of V_{GS}) becomes:

$$I_{Dsat} = \frac{g_0 V_{p0}}{3} + g_0(V_b - V_{GS})\left[\frac{2}{3}\sqrt{\frac{V_b - V_{GS}}{V_{p0}}} - 1\right] \tag{5.14}$$

For V_{GS}=0, we obtain the expression for the maximum saturation current:

$$I_{Dss} = \frac{g_0 V_{p0}}{3} + g_0 V_b\left[\frac{2}{3}\sqrt{\frac{V_b}{V_{p0}}} - 1\right] \tag{5.15}$$

Afterwards we can write:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 (1 - \lambda V_{DS}) \quad \textbf{(5.16)}$$

In practice, the transfer characteristic is often compared to a parabola ($\lambda \ll 0$) and the expression of the saturation current is very often given by the empirical relationship:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 \quad \textbf{(5.17)}$$

From the above equation we can deduce the expression for transconductance as:

$$g_m = -\frac{2}{V_P} I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right) \quad \textbf{(5.18)}$$

$$g_m = g_{m0}\left(1 - \frac{V_{GS}}{V_P}\right) \quad \textbf{(5.19)}$$

With $g_{m0} = -\frac{2}{V_P} I_{DSS}$

Noticed: The characteristics of p-channel JTFETs are similar to those of n-channel JTFETs. The latter are derived from the former by reversing all polarities, which in the analysis amounts to replacing all voltages with their opposites. P-channel JFETs are much less commonly used than n-channel JFETs because holes are less mobile than electrons, which give these JFETs a higher channel resistance.

U1897-U1899

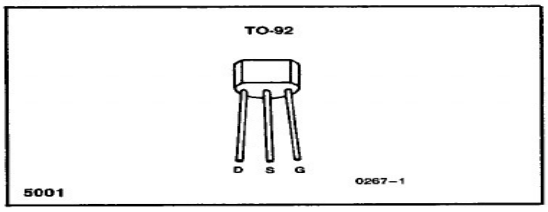
U1897–U1899
N–Channel JFET Switch

INTERSIL

FEATURES
- Low Insertion Loss
- No Error or Offset Voltage Generated By Closed Switch

APPLICATIONS
- Analog Switches, Choppers

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS
(T_A = 25°C unless otherwise noted)

Gate-Drain or Gate-Source Voltage	−40V
Forward Gate Current	10mA
Storage Temperature Range	−55°C to +150°C
Operating Temperature Range	−55°C to +135°C
Lead Temperature (Soldering, 10sec)	+300°C
Power Dissipation	350mW
Derate above 25°C	3.2mW/°C

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

ORDERING INFORMATION

TO-92	TO-92-18
U1897	U1897-18
U1898	U1898-18
U1899	U1899-18

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	U1897		U1898		U1899		Units
			Min	Max	Min	Max	Min	Max	
BV_{GSS}	Gate-Source Breakdown Voltage	I_G = −1μA, V_{DS} = 0	−40		−40		−40		V
I_{GSS}	Gate Reverse Current	V_{GS} = −20V, V_{DS} = 0		−400		−400		−400	pA
I_{DGO}	Drain-Gate Leakage Current	V_{DG} = 20V, I_S = 0		200		200		200	
I_{SGO}	Source-Gate Leakage Current	V_{SG} = 20V, I_D = 0		200		200		200	
$I_{D(off)}$	Drain Cutoff Current	V_{DS} = 20V, V_{GS} = −12V (U1897)		200		200		200	
		V_{GS} = −8V (U1898), V_{GS} = −6V (U1899), T_A = 85°C		10		10		10	nA
$V_{GS(off)}$	Gate-Source Cutoff Voltage	V_{DS} = 20V, I_D = 1nA	−5.0	−10	−2.0	−7.0-	−1.0	−5.0	V
I_{DSS}	Saturation Drain Current (Note 1)	V_{DS} = 20V, V_{GS} = 0	30		15		8.0		mA
$V_{DS(on)}$	Drain-Source ON Voltage	V_{GS} = 0, I_D = 6.6mA (U1897), I_D = 4.0mA (U1898), I_D = 2.5mA (U1899)		0.2		0.2		0.2	V
$r_{DS(on)}$	Static Drain-Source ON Resistance	I_D = 1mA, V_{GS} = 0		30		50		80	Ω

INTERSIL'S SOLE AND EXCLUSIVE WARRANTY OBLIGATION WITH RESPECT TO THIS PRODUCT SHALL BE THAT STATED IN THE WARRANTY ARTICLE OF THE CONDITION OF SALE. THE WARRANTY SHALL BE EXCLUSIVE AND SHALL BE IN LIEU OF ALL OTHER WARRANTIES, EXPRESS, IMPLIED OR STATUTORY, INCLUDING THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR USE.

NOTE: All typical values have been characterized but are not tested.

10-110

Figure 5.17: JFET **U1897-U1899** Datasheet

5.5.2 JFET Biasing Techniques

There are three main circuits used for JFET transistor biasing: Fixed polarization, self-polarization and polarization by resistance bridgen (divider bridge)

a. Fixed polarization

The fixed bias circuit is given opposite.

From the circuit we deduce:

- Source voltage equal to 0V: Vs=0V
- The output mesh: $V_{DS} = V_{DD} - R_D.I_D$
- The input mesh: $V_{GS} = -V_{GG}$

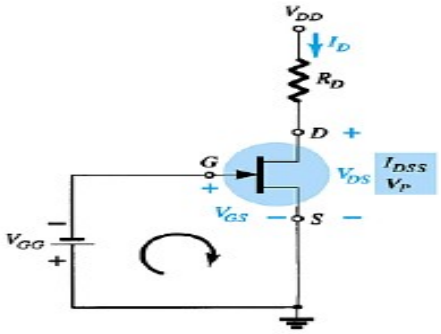


Fig 5.18 : JFET Fixed Bias Circuit

b. Self-polarization or automatic polarization

The circuit of the common source JFET self-bias is given below:

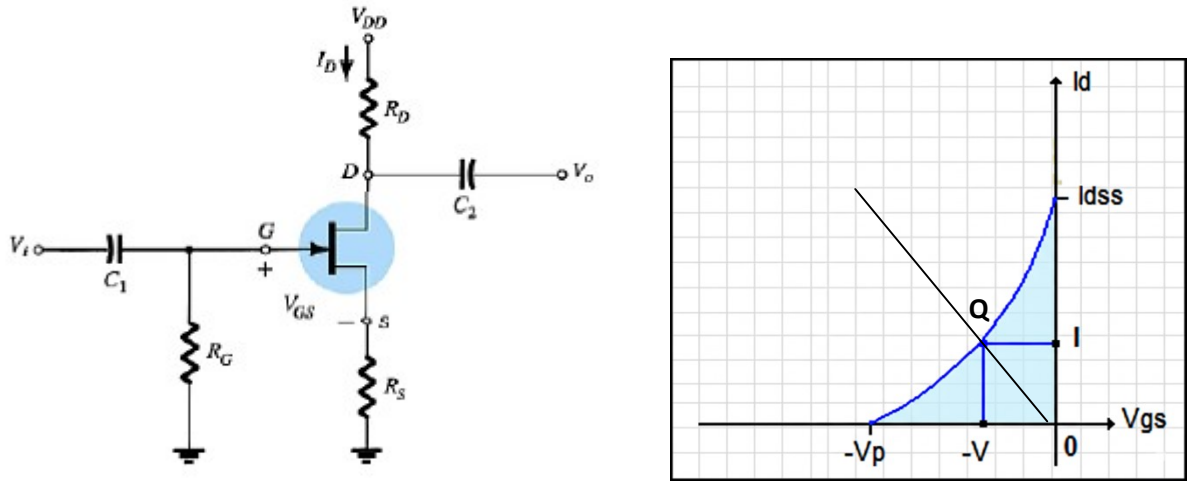


Figure 5.19: JFET self-bias circuit (left) and $I_d(V_P)$ characteristic (right)

For the input mesh: $V_{GS} = -I_D R_S$. So the gate-source junction is reverse biased. This equation is called the charge line equation.

To solve the equation and plot this line, we follow these steps:

i. We take two points:
- Point of origin which corresponds to I_D=0A therefore V_{GS}=0V
- Point which corresponds to $I_D = I_{DSS}$ (value provided by default) so we use the value of R_S (already known) we obtain V_{GS}.

ii. On the graph, display point Q identified by I_D and V_{GS}.

iii. We draw a line from the origin to this point.

iv. We draw the transfer curve, using I_{DSS} and V_P ($V_P = V_{GSoff}$ in the specifications) as well as some points on $I_D = \frac{I_{DSS}}{4}$ and $I_D = \frac{I_{DSS}}{2}$, etc.

The Q point (operating point) is located at the intersection of the load line and the transfer curve. The I_D value at the Q point (I_{DQ}) to solve for the other values:
For the output mesh:

- Output voltage: $\mathbf{V_o=V_{DS}+I_DR_S}$ **(5.20)**

$$\mathbf{V_{DS}=V_{DD}-I_D(R_S+R_D)} \quad \textbf{(5.21)}$$

c. Polarization by divider bridge

The JFET divider bridge biasing circuit is given below. This biasing mode is widely used. From the input mesh (see figure below), the voltage V_G is equal to the voltage across the voltage divider R_2:

$$V_G = \frac{R_2}{R_1+R_2}V_{DD} \quad \textbf{(5.22)}$$

$$V_{GS} = V_G - I_D R_S \quad \textbf{(5.23)}$$

To plot the curve in the figure above and determine the operating point Q, the following steps are followed:

- We draw the load line using two points/
  - $(V_{GS} = V_G\ ;\ I_D = 0A)$
  - $(V_{GS} = 0V\ ;\ I_D = \frac{V_G}{R_S}A)$
- We plot the transfer curve from I_D , V_p and the values of I_{DSS}calculated previously
- The operating point will therefore be the intersection of the two curves

Using the values of I_D at point Q, we can find the solutions for the other values:

$$V_{DS}=V_{DD}-I_D(R_S+R_D) \quad \textbf{(5.24)}$$

$$V_S=I_DR_S \quad \textbf{(5.25)}$$

$$V_D = V_{DD} - I_DR_D \quad \textbf{(5.26)}$$

$$I_{R1} = I_{R2} = \frac{V_{DD}}{R_1+R_2} \quad \textbf{(5.27)}$$

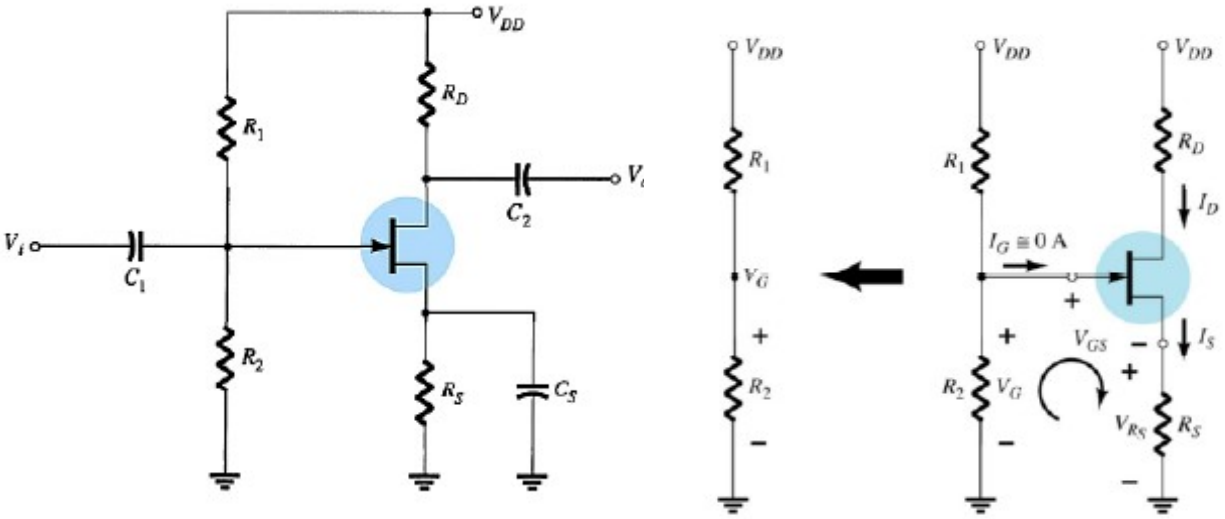


Figure 5.20: JFET Divider bridge bias circuit

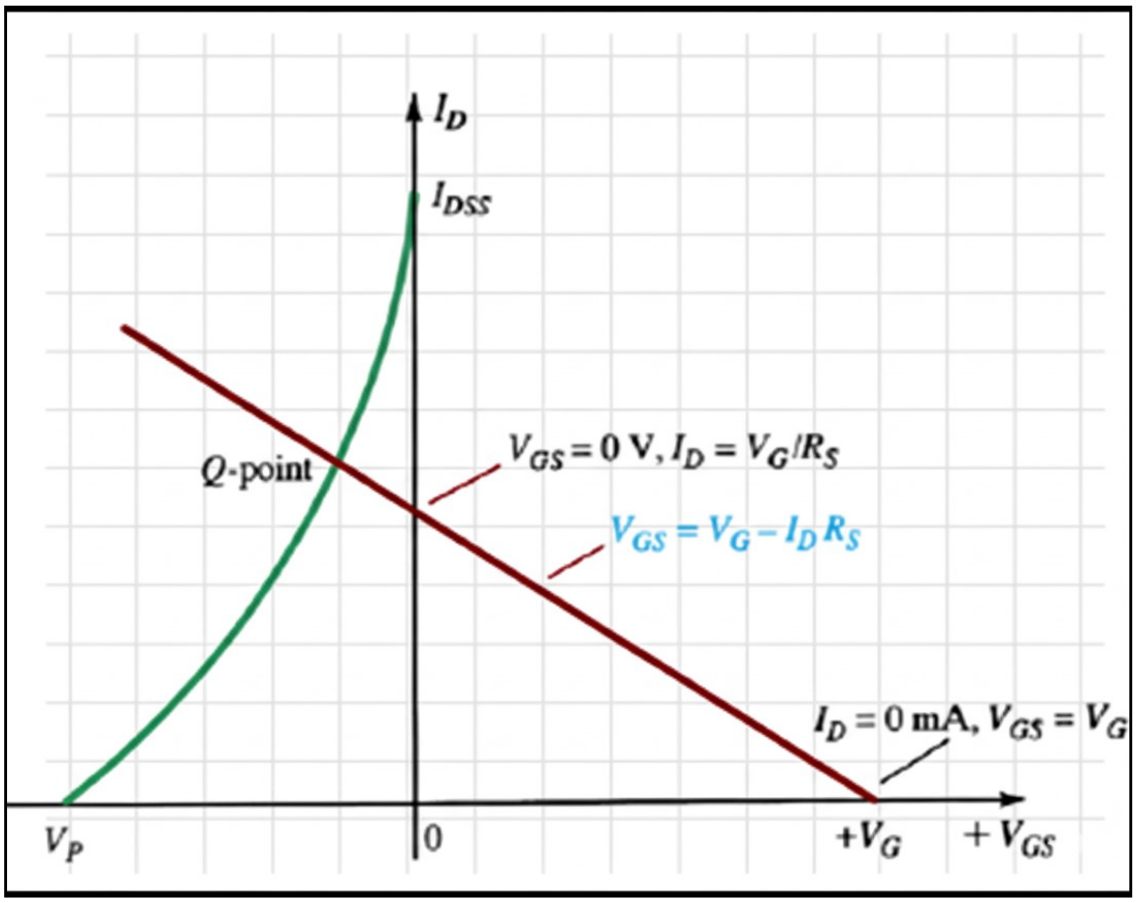


Figure 5.21: JFET transfert characteristic: $I_d(V_P)$

5.5.3 Comparison of Biasing Methods

Parameter	Fixed Gate Bias	Self-Bias	Voltage Divider Bias
Stability	Poor	Good	Excellent
Power Supplies	Two (V_{DD}, V_{GG})	One ($_{VDD}$)	One (V_{DD})
Component Count	Low (3-4)	Low (4-5)	Medium (5-6)
Q-point Control	Limited	Moderate	Excellent
Temperature Stability	Poor	Good	Excellent
Parameter Sensitivity	Very High	High	Low
Design Complexity	Simple	Moderate	Moderate
Practical Use	Rare (lab only)	Common (discrete)	Most Common (production)
Cost	Medium	Low	Medium
Suitability for Production	Poor	Fair	Excellent

***Table 5.1**: Comprehensive comparison of JFET biasing techniques*

5.5.4 Practical Biasing Considerations

a) **Device Selection:** In critical applications, JFETs may be selected or matched for specific I_{DSS} and V_P values to ensure consistent performance across production units.

b) **Temperature Compensation:** For applications requiring operation over wide temperature ranges, additional temperature compensation techniques may be employed, such as using temperature-dependent resistors or complementary temperature coefficients.

c) **Power Supply Variations:** Voltage divider bias provides the best immunity to power supply variations. Self-bias provides moderate immunity, while fixed bias is highly sensitive.

d) **Bypass Capacitor Selection:** The bypass capacitor value must be chosen based on the lowest frequency of operation. For audio applications, values of 10-100 µF are typical. For RF applications, smaller values may suffice.

e) **Gate Resistor Selection:** The gate resistor RG should be large enough to maintain high input impedance but not so large that it causes excessive DC offset due to gate leakage current. Values of 1to 10 MΩ are typical.

5.6 Common amplifier configurations - detailed analysis

5.6.1 Small-signal equivalent diagram

JFETs are inherently nonlinear devices, as described by the Shockley equation. While this equation accurately describes the DC behavior, it is cumbersome for analyzing the response to small AC signals. Small-signal models linearize the device behavior around a specific DC operating point (Q-point), allowing the use of linear circuit analysis techniques (such as superposition, Thevenin's theorem, and Norton's theorem) to predict amplifier performance. The small-signal model is valid only for small AC signal variations where the device's response can be approximated as linear. It provides a powerful tool for calculating key amplifier parameters:

- **Voltage Gain (Av)**
- **Current Gain (Ai)**
- **Input Impedance (Zin)**
- **Output Impedance (Zout)**
- **Frequency Response**

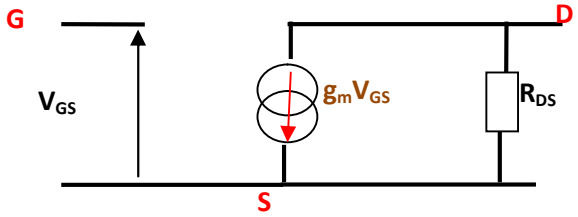


Figure 5.22: Small signal equivalent diagram

As for the bipolar transistor, the equivalent diagram concerns a suitably polarized component. Therefore operation is established in the pinch zone. The small-signal equivalent diagram of the N-channel JFET is as in figure 5.22. The lack of connection between the grid and source results in the very high grid-source impedance (considered infinite by approximation). At the output, we find the same elements as for the bipolar transistor: a current source controlled by the voltage V_{GS} (not by a current), as well as its parallel internal resistance R_{DS}. The resistance R_{DS} is very high (several hundred kΩ). In current applications this resistance is negligible (infinite and considered as open circuit in the assembly).

a) Common source assembly

The common-source configuration is the most widely used JFET amplifier, analogous to the common-emitter amplifier in BJT circuits. It provides high voltage gain, high input impedance, and moderate output impedance, making it ideal for general-purpose voltage amplification. By analogy, the common source assembly is the counterpart of the common emitter assembly for the bipolar transistor, therefore a similar operation. A common drain assembly also exists, which is the counterpart of the common collector assembly of the bipolar; this assembly is however of little interest, because the FET is a component with very high input impedance, and this, as we will see, even when it is used as a common source.

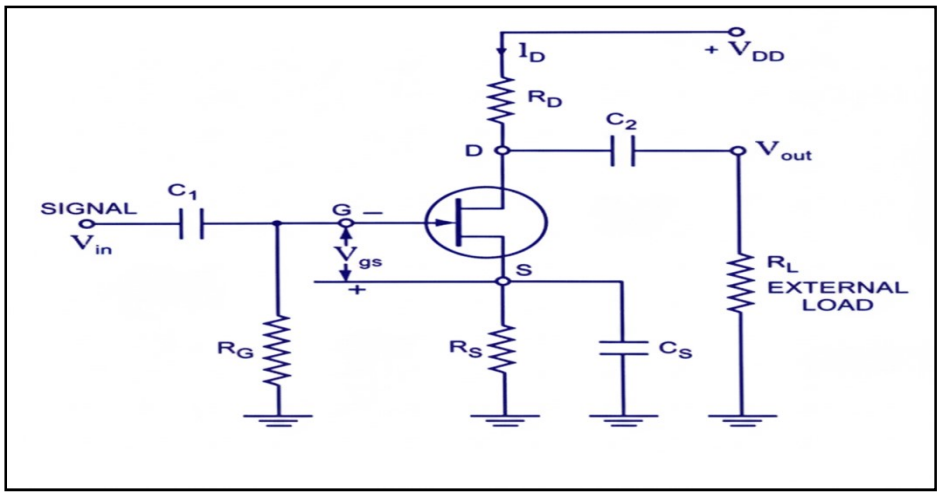


Figure 5.23: Common source assembly

Based on the small-signal equivalent diagram of the N-channel JFET, we can deduce this from the common-source assembly. To do this, we place the equivalent diagram of the JFET and then the other components: R_G, V_e, R_D and Vs in parallel on either side of the diagram.

Noticed: Since the assembly is a common source, then the resistor R_S will be shorted by the decoupling capacitor C_D.

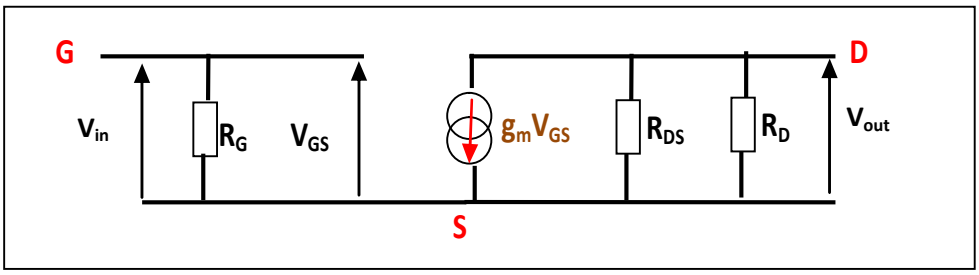
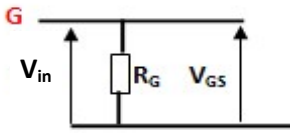


Figure 5.24: Small-signal equivalent diagram of the common source assembly

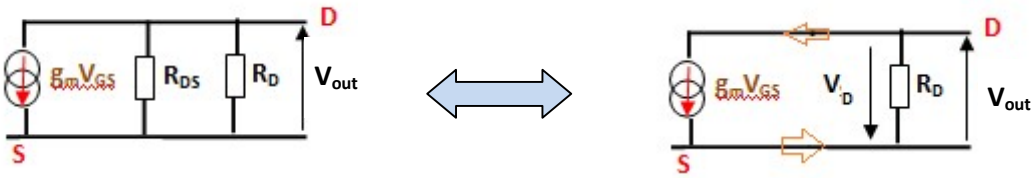
From the equivalent diagram we can deduce the following parameters:

iii. No-load voltage gain

- **Input voltage:** $V_{in}=V_{GS}$



- **Output voltage:** Neglecting R_{DS}, which has a very high value compared to R_D, we obtain:



In this case we can write:

$$V_D=g_m V_{GS} R_D \quad (5.28)$$

$$V_{out}= - V_D = -g_m V_{GS} R_D \quad (5.29)$$

So the no-load voltage gain (without load at the output of the assembly) is:

$$A_V = \frac{V_{out}}{V_{in}} = -\frac{g_m V_{GS} R_D}{V_{GS}} \quad (5.30)$$

$$A_V = -g_m V_{GS} \quad (5.31)$$

- **Input impedance**

From the input of the equivalent diagram we see that only the R_G resistor is at the input. As a result:

$$Z_{in} = R_G \quad (5.32)$$

Noticed: Care must be taken not to select a value that is excessively high. The resistor should be large enough that the voltage drop due to grid leakage current remains negligible. In practice, a value on the order of a few megaohms (MΩ) is typically used.

- **Output impedance:** Similarly looking at the output of the schematic, and approximating that R_{DS} is infinite, so the output impedance will be:

$$Z_{out} = R_D \quad (5.33)$$

Noticed: This value is average, R_D typically being worth a few kΩ. This assembly will generally not be able to be used without a downstream impedance matching stage.

- **Current Gain**

The current gain is the ratio of output current to input current. Since the gate draws negligible current:

$$A_i = \frac{I_{out}}{I_{in}} \cong \infty \quad (5.34)$$

In practical terms, the current gain is limited by the biasing resistors:

$$A_i \approx \frac{Z_{in}}{R_L} \quad (5.35)$$

Regarding the power gain, it is the product of voltage and current gains:

$$A_i = |A_v| x A_i \quad (5.36)$$

Its typical value varies from 1000 to 10,000 (30 to 40 dB).

The Miller effect is particularly significant in common-source amplifiers. The gate-drain capacitance C_{gd} appears multiplied by the voltage gain at the input, creating an effective input capacitance:

$$C_{in(Miller)} = C_{GD}(1 + |A_v|) \quad (5.37)$$

This characteristic limits the high-frequency response and bandwidth.

Some Applications

- Audio preamplifiers
- Instrumentation amplifiers
- RF amplifiers (with tuned load)
- General-purpose voltage amplification
- Input stages of multi-stage amplifiers
- Buffer amplifiers with gain and as sensor signal conditioning

Some design considerations

- Choose Q-point for maximum linear signal swing
- Bypass capacitor CS must be large enough for lowest frequency
- Coupling capacitors must not introduce excessive phase shift
- Load resistance affects gain and output impedance
- Trade-off between gain and bandwidth (Miller effect)
- Consider using cascode configuration for improved bandwidth

5.6.2 Common drain assembly (source follower)

The common-drain amplifier, universally known as a **source follower**, is analogous to the emitter follower in BJT circuits. It is characterized by unity voltage gain, very high input impedance, and very low output impedance, making it ideal for impedance matching and buffering applications.

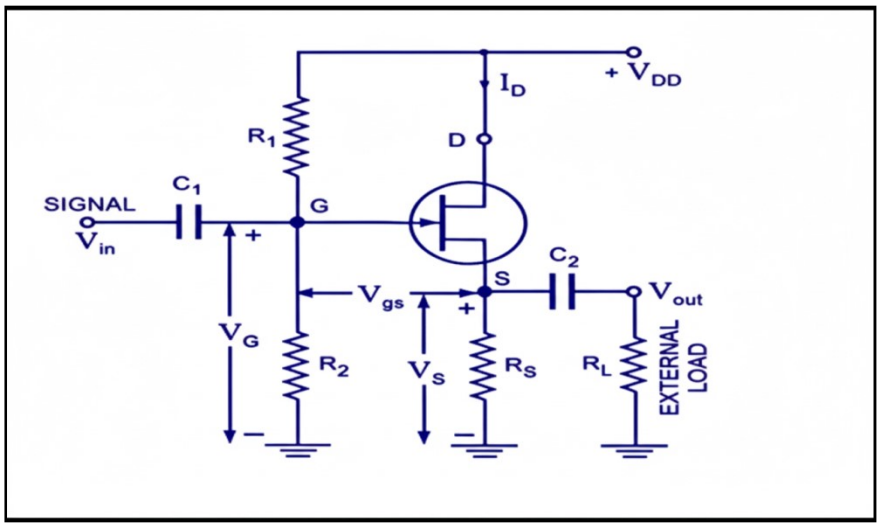


Figure 5.25: Common-drain JFET amplifier (source follower) showing the output taken from the source terminal

- **Circuit Configuration**

  - Input signal applied to gate through coupling capacitor
  - Output taken from source terminal
  - Drain terminal connected directly to V_{DD} (AC ground)
  - No drain resistor R_D
  - Source resistor R_S serves as load resistor
  - Biasing typically by voltage divider at gate

- **Operating Principle**

The key characteristic of the source follower is that the output voltage at the source "follows" the input voltage at the gate, hence the name. The output is in phase with the input (no phase inversion) and has a magnitude slightly less than the input.

The DC biasing is typically accomplished using voltage divider bias:

- Gate voltage: $V_G = V_{DD}\frac{R_2}{R_1+R_2}$
- Source voltage: $V_S = I_{DQ}R_S$
- Gate-source voltage: $V_{GSQ} = V_G - V_S$
- Drain-source voltage: $V_{DSQ} = V_{DD} - V_S = V_{DD} - I_{DQ}R_S$

Note: The Q-point must satisfy: $V_{DSQ} > |V_{GSQ} - V_P|$ to ensure saturation region operation.

- **AC analysis (small-signal)**

Input Impedance: The input impedance is determined by the voltage divider:

$Z_{in} = R_1||R_2$

Its typical value range from 100 kΩ to 10 MΩ, providing excellent input buffering.

Output Impedance: The output impedance looking into the source is remarkably low:

$$Z_{out} = R_S||(\frac{1}{g_m}) \quad (5.38)$$

For typical values where $R_S \gg \frac{1}{g_m}$: $Z_{out} \approx \frac{1}{g_m}$

Typical values: 100Ω to 1kΩ, making the source follower an excellent low-impedance driver.

Voltage Gain: The voltage gain of the source follower is:

$$A_v = \frac{g_m(R_S||R_L)}{1+g_m(R_S||R_L)} \quad (5.39)$$

This can be rewritten as:

$$A_v = \frac{1}{1+\frac{1}{g_m(R_S||R_L)}} \quad (5.40)$$

For large g_m and moderate R_S: $A_v \approx \frac{R_S}{R_S+\frac{1}{g_m}}$

In the limit where $g_m \gg 1$: $A_v \approx 1$

Notes: Typical values: 0.8 to 0.99, approaching unity but always less than 1.

The key point is that the voltage gain is positive (no phase inversion) and close to unity.

Current Gain: The current gain is substantial because the gate draws negligible current while the source can supply significant current:

$$A_i = \frac{Z_{in}}{R_S||R_L} \tag{5.41}$$

Its typical value range from: 100 to 1000.

Power Gain: Despite unity voltage gain, the source follower provides significant power gain due to its high current gain:

$$A_p = A_v A_i \approx A_i \tag{5.42}$$

For the common-gate configuration is analogous to the common-base amplifier in BJT circuits. It is characterized by low input impedance, high output impedance, high voltage gain, and no phase inversion. While less commonly used than common-source or common-drain configurations, it offers unique advantages for specific applications, particularly at high frequencies.

- **Voltage Gain:** Av = gm × RD (positive, no inversion)
- **Input Impedance:** Zin ≈ 1/gm (very low)
- **Output Impedance:** Zout ≈ RD (high)
- **Current Gain:** Ai ≈ 1
- **Phase Shift:** 0° (no inversion)

- **Comparison of JFET amplifier configurations**

The following table provides a comprehensive comparison of the three basic JFET amplifier configurations:

Parameter	Common-source	Common-drain	Common-gate
Voltage Gain (Av)	High (10-100)	≈ 1 (0.8-0.99)	High (10-100)
Current Gain (Ai)	Very High	Very High	≈ 1
Power Gain (Ap)	Very High	High	Medium
Input Impedance	Very High (MΩ)	Very High (MΩ)	Very Low (Ω)
Output Impedance	Medium (kΩ)	Very Low (Ω)	High (kΩ)
Phase Shift	180°	0°	0°
Frequency Response	Good	Excellent	Excellent
Miller Effect	Significant	Minimal	None
Bandwidth	Moderate	Wide	Very Wide
Reverse Isolation	Poor	Good	Excellent
Typical Applications	Voltage Amplification	Buffer/Impedance Matching	High-Freq/Cascode
Distortion	Moderate	Low	Moderate
Noise Figure	Low	Low	Low
Complexity	Medium	Simple	Medium

Table 5.2: Comparison of JFET amplifier configurations

References

1. Sze, S. M., & Ng, K. K. (2007). *Physics of semiconductor devices* (3rd ed.). Wiley-Interscience.
2. Streetman, B. G., & Banerjee, S. (2015). *Solid state electronic devices* (7th ed.). Pearson.
3. Kittel, C. (2005). *Introduction to solid state physics* (8th ed.). Wiley.
4. Neamen, D. A. (2012). *Semiconductor physics and devices* (4th ed.). McGraw-Hill.
5. Pierret, R. F. (1996). *Semiconductor device fundamentals*. Addison-Wesley.
6. Boylestad, R. L., & Nashelsky, L. (2013). *Electronic devices and circuit theory* (11th ed.). Pearson.
7. Sedra, A. S., & Smith, K. C. (2021). *Microelectronic circuits* (8th ed.). Oxford University Press.
8. Gray, P. R., Hurst, P. J., Lewis, S. H., & Meyer, R. G. (2009). *Analysis and design of analog integrated circuits* (5th ed.). Wiley.
9. Millman, J., & Grabel, A. (1987). *Microelectronics* (2nd ed.). McGraw-Hill.
10. Tsividis, Y. (1999). *Operation and modeling of the MOS transistor* (2nd ed.). Oxford University Press.
11. Sedra, A. S., & Smith, K. C. (2015). Microelectronic circuits (7th ed.). Oxford University Press.
12. Millman, J., & Grabel, A. (1987). Microelectronics (2nd ed.). McGraw-Hill.
13. Gray, P. R., Hurst, P. J., Lewis, S. H., & Meyer, R. G. (2009). Analysis and design of analog integrated circuits (5th ed.). Wiley.
14. Horowitz, P., & Hill, W. (2015). The art of electronics (3rd ed.). Cambridge University Press.
15. Ebers, J. J., & Moll, J. L. (1954). Large-signal behavior of junction transistors. Proceedings of the IRE, 42(12), 1761–1772.